Dual 16 bit 44 kHz Multiplexed D/A Converter

Description

The CX20133 is a 16 bit D/A converter IC for PCM audio using the integrating formula. Analog signal is reproduced from the 16 bit digital signal by combining an integrator, analog switch and low-pass filter to the IC exterior. Following circuits are also built-in.

- Integrating current output
- Two channels of discharge signal output
- Level shifting for interface direct with TTL/MOS LSIs.
- Analog switch drive.

Features

- Miniature flat package requires only small mounting area.
- Conversion frequency of 44.1 kHz.
- Serial data input.
- Low distortion factor typically at 0.003%.

Structure

- Bipolar Silicon Monolithic IC

Absolute Maximum Ratings (Ta = 25°C)

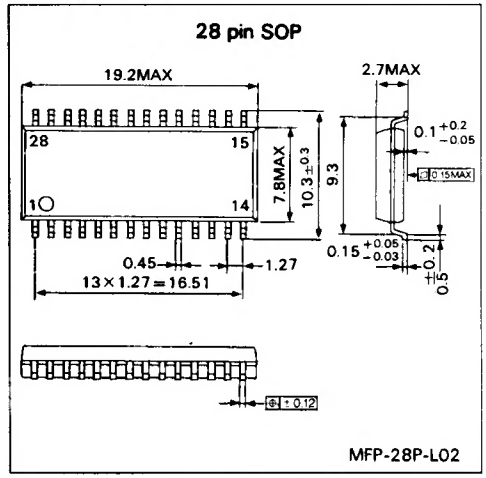
• Supply voltage	V_{CC} to V_{EE}	12	V
• Operating temperature	T_{opr}	−10 to +75	°C
• Storage temperature	T_{stg}	−50 to +125	°C
• Allowable power dissipation	P_D	1.1	W

Recommended Operating Conditions

• Supply voltage	V_{CC}	5 ± 0.25	V
	V_{EE}	−5 ± 0.25	V

Package Outline

Unit: mm



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Block Diagram

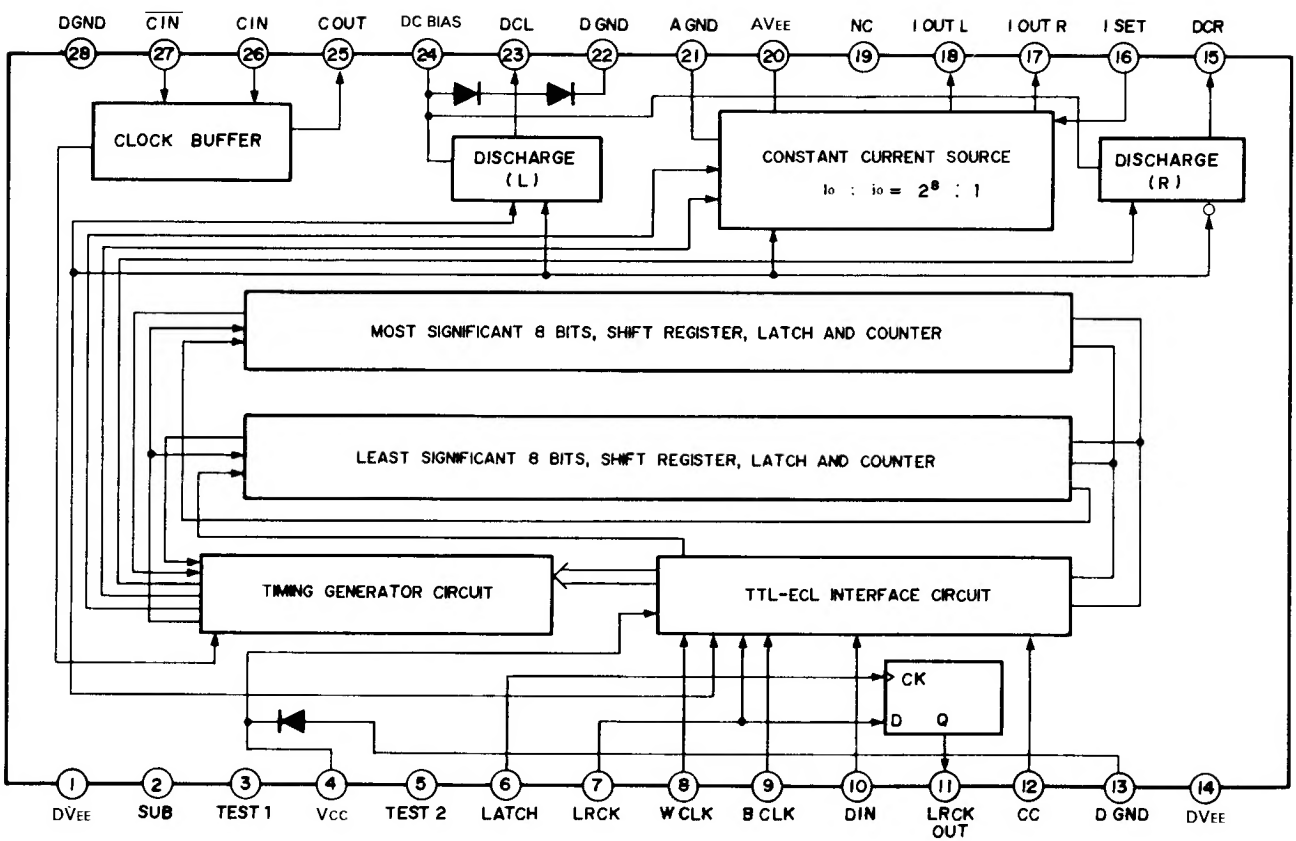


Fig. 1

SONY

Pin Description

No.	Symbol	Description
1	DV_{EE}	Power supply pin for the digital circuit. Applied with −5 V.
2	SUB	IC substrate. Always connected to 1 pin.
3	TEST 1	Test pin, normally open.
4	V_{CC}	Power supply pin for the digital circuit. Applied with +5 V.
5	TEST 2	Test pin, normally open.
6	LATCH	Clock pin of D-type clutch.
7	LRCK	LRCK input pin.
8	WCLK	WCLK input pin.
9	BCLK	BCLK input pin.
10	DIN	DIN (data input pin).
11	LRCK OUT	LRCK output pin.
12	CC	CC input pin.
13	DGND	Ground pin for the digital circuit.
14	DV_{EE}	Power supply pin for the digital circuit. Applied with −5 V.
15	DCR	Output pin of R-channel discharge driving signal.
16	ISET	Pin for setting integration current.
17	IOUTR	Output pin for R-channel current.
18	IOUTL	Output pin for L-channel current.
19	NC	No connection.
20	AV_{EE}	Power supply pin for the analog circuit.
21	AGND	Ground pin for the analog circuit.
22	DGND	Ground pin for the digital circuit.
23	DCL	Output pin for L-channel discharge driving signal.
24	DCBIAS	Bias pin for the discharge circuit.
25	COUT	Output pin for the clock oscillator.
26	CIN	Positive input pin for the clock oscillator.
27	$\overline{CIN}$	Negative input pin for the clock oscillator.
28	DGND	Ground pin for the digital circuit.

Electrical Characteristics

(Ta = 25°C, V_{EE} = −5.0V, V_{CC} = 1.0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Circuit current	I_{EE}	1, 2, 14, 20	−112	−85		mA	1
Circuit current	I_{CC}	4		9.5	12.5	mA	1
Input threshold voltage	V_{TH}	6, 7, 8, 9, 10, 12		2.1		V	
High-level input voltage	V_{IH}	6, 7, 8, 9, 10, 12	2.8			V	
Low-level input voltage	V_{IL}	6, 7, 8, 9, 10, 12			0.8	V	
High-level input current	I_{IH}	6, 7, 8, 9, 10, 12 V_{IH} = 4.5V			500	μA	
Low-level input current	I_{IL}	6, 7, 8, 9, 10, 12 V_{IL} = 0V			500	μA	
High-level output voltage	V_{LRCKH}	11 Pin 7 = 4.5V I_{OH} = −100μA Pin 6:1 clock input:0V−5V−0V	2.7			V	
Low-level output voltage	V_{LRCKL}	11 Pin 7 = 0V I_{OL} = 100μA Pin 6:1 clock input: 0V−5V−0V			−2.7	V	
Clock input bias voltage	V_{CIN}	26, 27		−1.3		V	
Clock high-level output voltage	V_{CCR}	25		−0.8		V	
Clock low-level output voltage	V_{COL}	25		−1.6		V	
Current output pin leak	$I_{O\ LEAK}$	17, 18 Pins 17, 18: voltage = 0V when current output is off.			1.5	μA	
I_{OUT} output current	I_{OUT}	17, 18 Pins 17, 18: voltage = 0V Pin 16 I_{SET} = 500μA (I_{OUT} = Io − io)		2.00B		mA	
Current ratio*1	Io/io	17, 18 Pin 16 I_{SET} = 250μA	255.0	256.0	257.5	−	2
Discharge circuit current dissipetion	I_{OC}	24 Set Pin 24 to 0V.	1.35	1.9	2.5	mA	
Discharge circuit high-level output voltage	V_{DCH}	15, 23 Pin 24 voltege = 1.4V Load current = −100μA	0.27	0.45	0.77	V	
Discharge circuit low-level output voltage	V_{DCL}	15, 23 Pin 24 voltage = 1.4V Load current = −100μA		−4.2	−3.5	V	
Maximum I_{SET} current	$I_{SET\ MAX}$	16 In the renge when the $I_{OUTL(R)}$ current ratio satisfies 255<Io/io<257			575	μA	
Distortion factor	THD	Both right end left, 0dB (full scale) reproduction 680Hz		0.003	0.005	%	3
		8oth right and left, −20dB reproduction 680Hz		0.02	0.025	%	3
Operating clock frequency	f_{CLK}	Self-ectivating/Activeted			36	MHz	

Note 1) Ground Pins 13, 17, 18, 21, 22, 24 and 28. Connect Pin 16 via a resistor of 5.1 kΩ and keep other pins open.

2) Io and io must satisfy the relation below in the Current Ratio Test Circuit (Fig. 3):
$-3.9\ (mV) < 1\ (k\Omega) \times Io\ (\mu A) - 256\ (k\Omega) \times io\ (\mu A) < 5.9\ (mV)$

3) See the Test Circuit (Fig. 2).
Conversion frequency: 44.1 kHz
Input data: Use the 16 bit full-scale data (0 dB) generated by the data generator.
Distortion meter: Use the HP339A (with all filters on) or the like provided with 80 kHz LPF, 30 kHz LPF and 400 Hz HPF.

*1 In the Current Ratio Test Circuit (Fig. 3),
$-3.9(mV) < 1(k\Omega) \times Io(\mu A) - 256(k\Omega) \times io(\mu A) < 5.9(mV)$

Description of the Conversion Operation

(1) Data call (BCLK, DIN, WCLK, LRCK). Refer to Fig. 1.

The data comes in 16 bit serial signal with 2's compliment. The data is sent sequencially into the IC beginning from MSB in sync with the rise of the bit clock (BCLK). (The data change represents the BCLK fall).

When the word clock (WCLK) is changed from the high-level to low-level at the 17th fall of BCLK, the 16 bit data is transferred from the shift register to the latch by the fall signal.

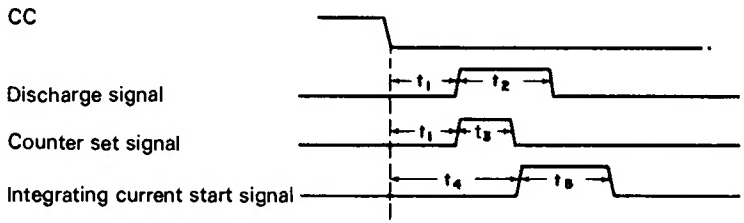
When the CX20133 is used in the stereo mode, data from other channels are sent in from the 17th BCLK.

In the stereo mode, Rch data is called when LRCK at the low level and Lch data is called in when the LRCK is at the high level. IOUTL and DCL operate only when LRCK is at the low level and IOUTR and DCR operate only when LRCK is at the high level.

(2) Conversion operation (CC, LRCK, CIN, IOUTL, IOUTR, DCL, DCR)

When more than 3 clocks are input from the clock input (CIN) with conversion command at the high level, all inner timing circuits are reset.

After resetting, the inner timing circuit starts operation when a clock is input from CIN with CC at the low level. The three signal generated this way are the discharge signal, counter set signal and integrating signal. Time of these three signals is determined depending on the clock cycle and their number of quantity:



$t_1 = 34 \times \tau_0$
$t_2 = 67 \times \tau_0$
$t_3 = 31 \times \tau_0$
$t_4 = 65 \times \tau_0$
t_5 Min $= 45 \times \tau_0$ (input data 01 to 1)
t_5 Max $= 302 \times \tau_0$ (input data 10 to 0)

The counter set signal is to set the data input to the latch to the counter and it is not output externally.

The discharge signal is output from DCL and DCR and it is controlled by LRCK. It is output from DCL when LRCK is at the low level and from the DCR when LRCK is at the high level.

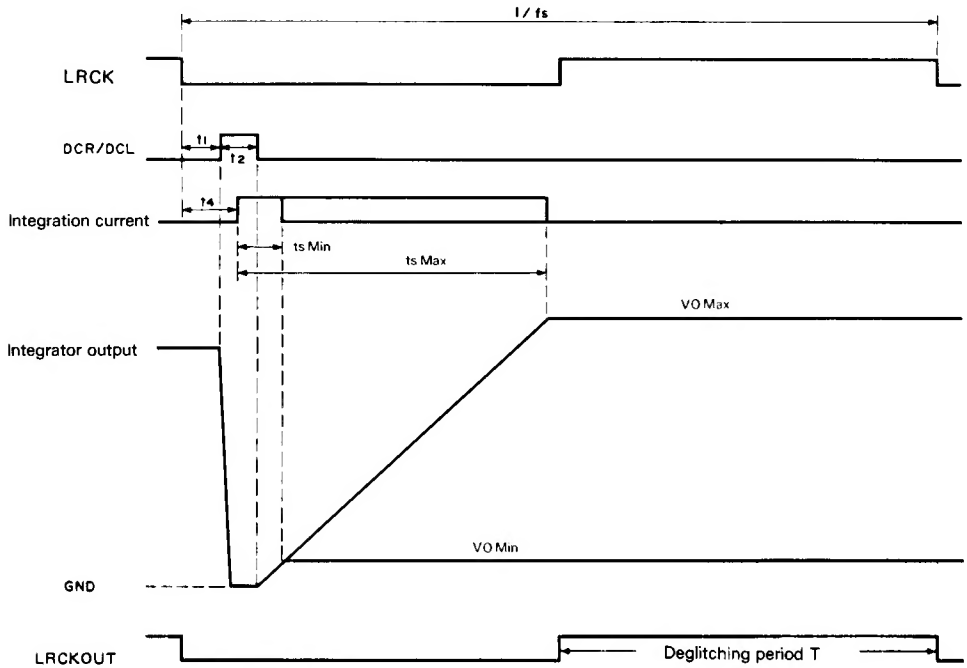
By the integrating current start signal, the upper current Io and lower current io start flowing. The counter starts counting from the preset value simultaneously when the discharge signal is off, measures the 11 offsets after completion of counting and outputs a signal to stop the integrating current.

The t5 value is varied between 0 and 255 by the preset input data in the counter.

Therefore, the conversion time from the start of low CC level to the completion of integrating requires t4 + t5 sec max.

The integrating current, like the discharge signal, is controlled by LRCK; IOUTL is output when LRCK is at the low level and IOUTR is output when LRCK is at the high level.

The Relation between Sampling Frequency fs and Clock



The maximum and minimum values of the integration voltage output, V_O Max and V_O Min, are expressed as follows:

$$V_O\,Max = \frac{I_O}{C} * \tau_O * 267 + \frac{i_O}{C} * \tau_O * 266 \qquad (t_4 + t_5\,Max)$$

$$V_O\,Min = \frac{I_O}{C} * \tau_O * 12 + \frac{i_O}{C} * \tau_O * 11 \qquad (t_4 + t_5\,Min)$$

where f_{CLK} is a clock frequency and τ is a period.

The integration voltage is held by the capacitor C in the integrator when the current is switched off. This voltage is used as D/A conversion output during the deglitching period T which is given according to the settling time of the deglitching circuit.

The relation between the conversion frequency fs and the clock frequency f_{CLK} is given as below assuming that the conversion time and deglitching period are equivalent:

$$fs = \frac{f_{CLK}}{2 \times (t_4 + t_5\,Max)} = \frac{f_{CLK}}{734}$$

where fs=44.1 kHz results in 32.4 MHz of f_{CLK}.

It is, however, recommendable to specify fs as the follow for the practical use because a settling time of 0.5 to 1.0 μs is required for the integrator after the current for t_5 disappears:

$$fs = \frac{f_{CLK}}{2(t_4 + t_5\,Max + 1.0\,(\mu s)) + T}$$

(3) Integration current setting (ISET, IOUTL, LOUTR)

Integration current is determined by a constant current value input through the ISET pin, which is given as below:

$$\text{IOUTL (R)} = I_o + i_o$$
$$= (4 + \frac{1}{64}) \text{ ISET}$$

where i_o and I_o are integration currents corresponded to the ILSB and 2^8LSB, respectively.

If D_0 and D_{15} are specified as MSB and LSB, respectively, integrator output voltage V_o is given by the following equation:

$$V_o = \frac{I_o}{C} (D_0 * 2^7 + \overline{D}_1 * 2^7 + \cdots\cdots + \overline{D}_7 * 2^0 + 12)\, \tau_0$$
$$+ \frac{i_o}{C} (\overline{D}_8 * 2^7 + \overline{D}_9 * 2^6 + \cdots\cdots + \overline{D}_{15} + 2^0 + 11)\, \tau_0$$

where $I_{SET} = 500\mu A$, $\tau_0 = \frac{1}{35\ (MHz)} = 28.6$ (ns) and $C = 2000$ pF result in the maximum output voltage V_o Max of the integrator when any of a value from 10 to 0 is given as an input data. Based on the relations below,

$I_o = 4 \cdot I_{SET}$

$i_o = \frac{1}{64} \cdot I_{SET}$,

V_o Max is calculated as the follow:

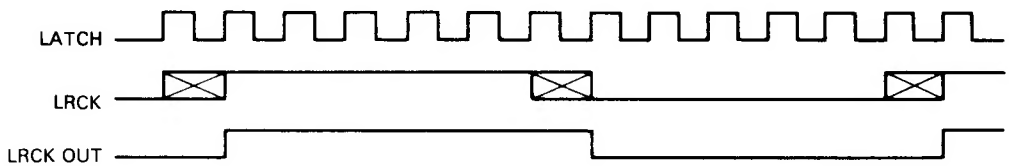
$$V_o \text{ Max} = \frac{2.0 \times 10^{-3}}{2000 \times 10^{-12}} * 267 * 28.6 \times 10^{-9}$$
$$+ \frac{500 * 10^{-6}/64}{2000 \times 10^{-12}} * 266 * 28.6 \times 10^{-9}$$
$$= 7.67 \text{ (V)}$$

(4) Operation of LRCK OUT

The LRCK OUT is an output for the analog switch IC (equivalent to MC14053B) drive to clip the output converted by the CX20133 and integrator as a PAM wave.

A PAM wave jitter may cause a conversion error and a D-type flip-flop is incorporated to eliminate this jitter; the LATCH input is used as a clock for the flip-flop.

This D-type flip-flop changes the output status in sync with the clock rise. The LRCK OUT operates only when +5 V is applied to Vcc. The output voltage level ranges from −2.7 V to +2.7 V enough to drive the CMOS analog switch effectively.



Timing of LATCH, LARCK and LRCKO

(5) Clock input/output pin (COUNT, CIN, $\overline{\text{CIN}}$)

The clock buffer consists of a circuit equivalent to a general-purpose ECL logic circuit, with its input pin biased by the internal bias circuit. The (≈ -1.3 V) output amplitude level is 0.8 V.

(6) Bias pin (DVEE, SUB, DGND, VCC, AVEE, AGND, DC BIAS)

SUB is used at the common potential with DVEE. A standard value for the DVEE and AVEE is -5.0 V.

The CX20133 is devised so that it can operate when voltage at the digital input pin has a value between either 0 to -5 V or 0 to $+5$ V. When operated with an input between 0 and $+5$ V, $+5$ V must be applied to VCC. In this case, LRCK OUT is output as mentioned above.

When operated with an input between 0 to -5 V, VCC must be set open.

DC BIAS is for the bias circuit of the discharge signal output circuit. Supply current of (2.5 mA $+\alpha$) from a power supply of $+5$ V or above, because this pin requires approx. 2.5 mA current as a standard value. The potential at the pin is biased at 2 Vf.

A value α can be determined according to the following procedures. Approx. 0.5 mA current is necessary to retain 2 Vf (approx. 1.4 V) at this pin. The maximum current that flows through the load resistor RL attached to DCR (15 Pin) and DCL (23 Pin) is calculated as the follow:

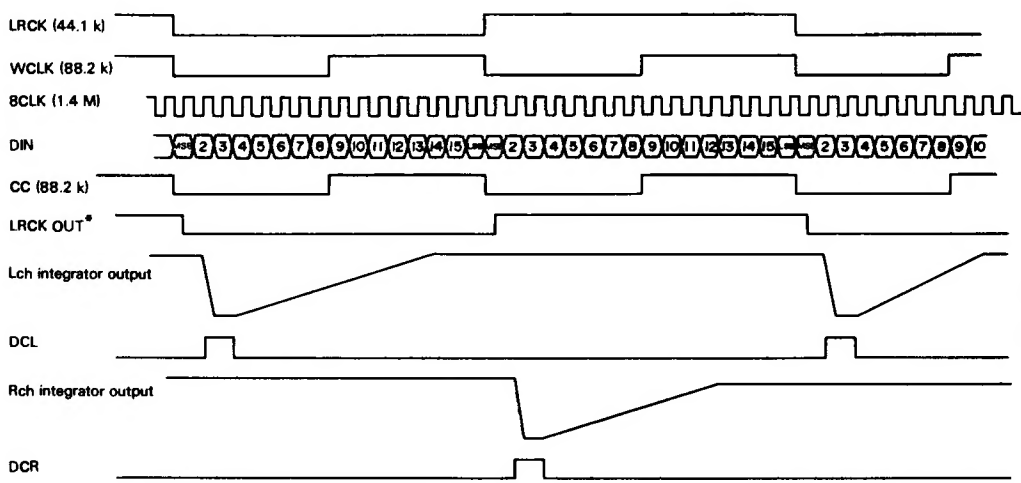
$$1/R_L \times (V_{DCH} + |DV_{EE}|)$$

The above equation results in 1.15 V where $R_L = 4.7\ k\Omega$, $V_{DCH} = 0.4$ V and $DV_{EE} = -5$ V are specified. Then α is calculated as

$$\alpha = 0.5 + 1.15 = 1.65\ (mA),$$

and required current is then obtained as 4.15 mA. Recommended value is 5 mA for $R_L = 4.7\ k\Omega$.

Timing Chart in the Stereo Mode



* When LATCH input is used as BCLK.

Fig. 1

Application Circuit and Test Circuit

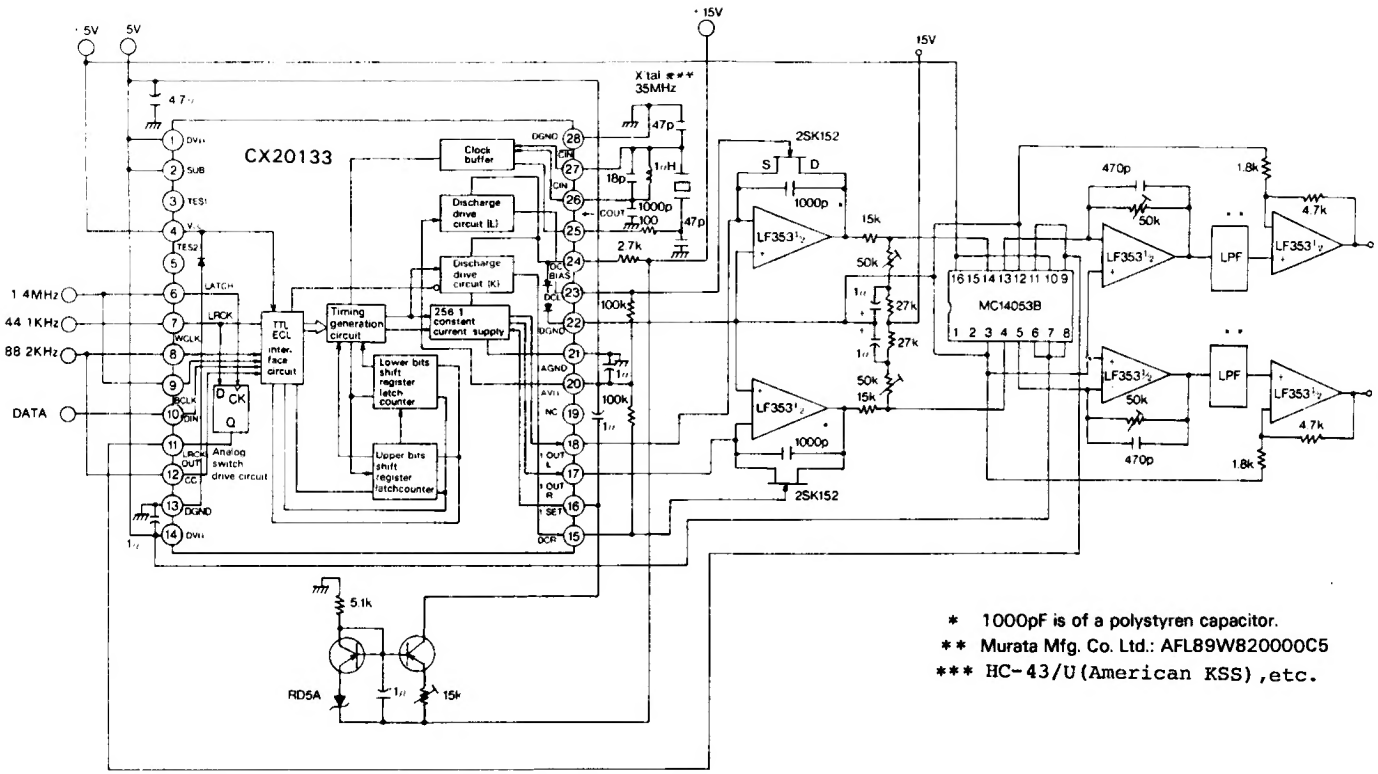
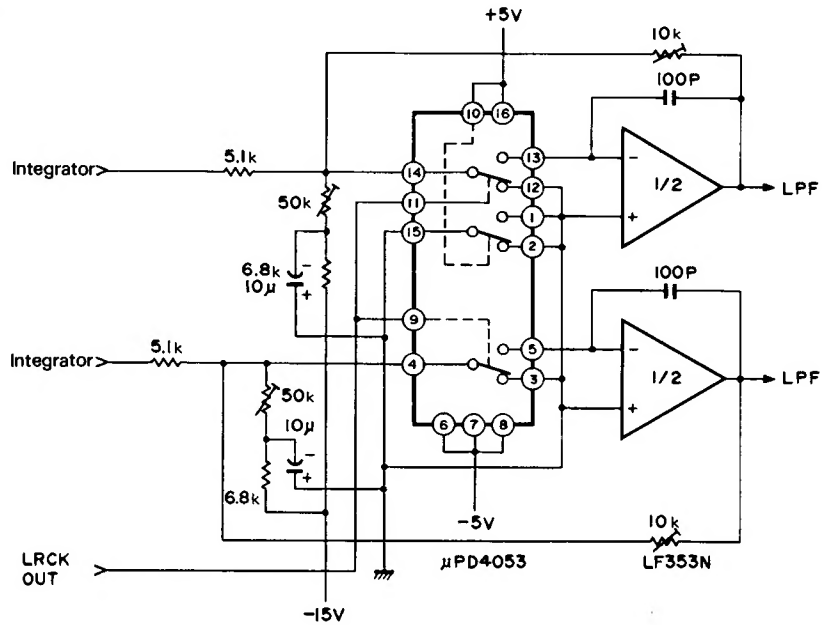


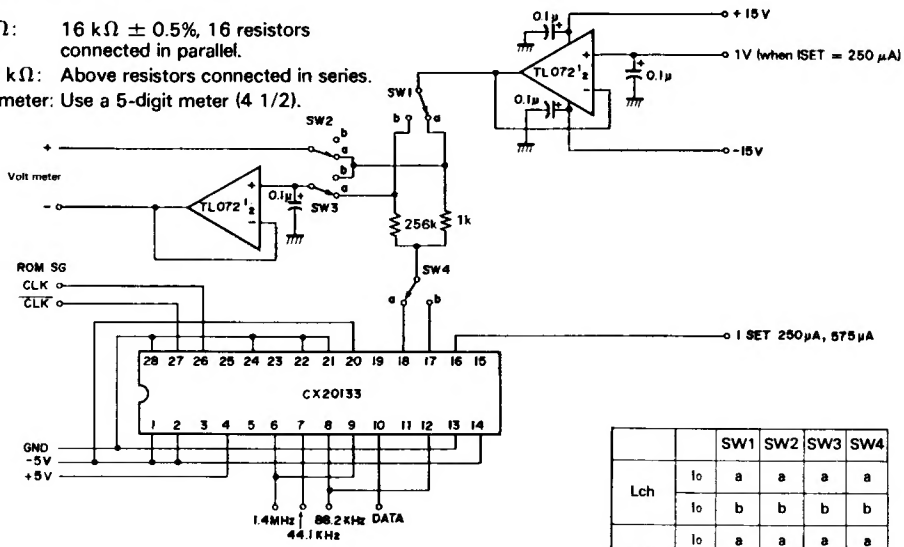
Fig. 2

Sample/Hold Circuit for Deglitching



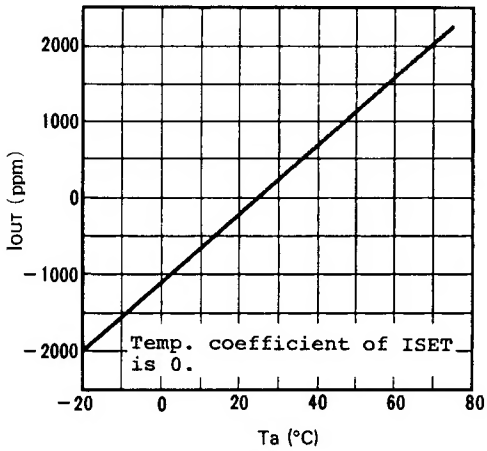
Current Ratio Test Circuit

1 kΩ: 16 kΩ ± 0.5%, 16 resistors connected in parallel.
256 kΩ: Above resistors connected in series.
Voltmeter: Use a 5-digit meter (4 1/2).

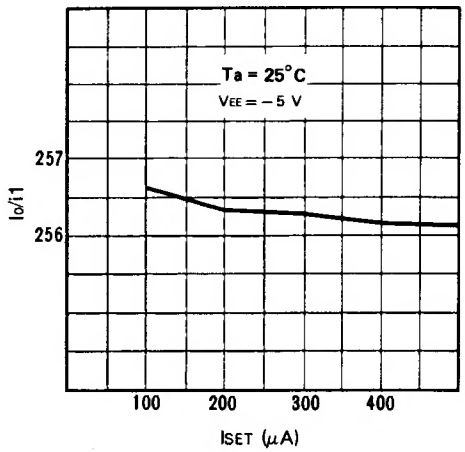


		SW1	SW2	SW3	SW4
Lch	Io	a	a	a	a
	Io	b	b	b	b
Rch	Io	a	a	a	a
	Io	b	b	b	b

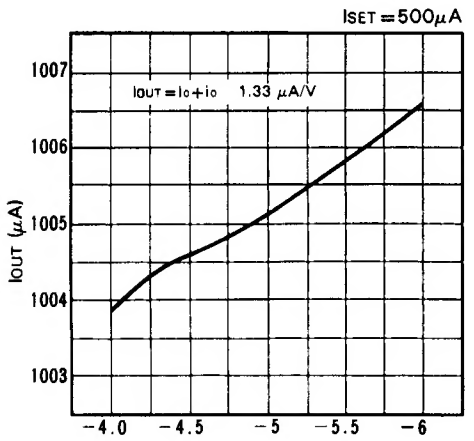
Temperature characteristics of I_{OUT} (I_O+i_O) (R, Lch common)



I_O/i_O vs. I_{SET}



Output current vs. Supply voltage (V_{EE})



Distortion factor