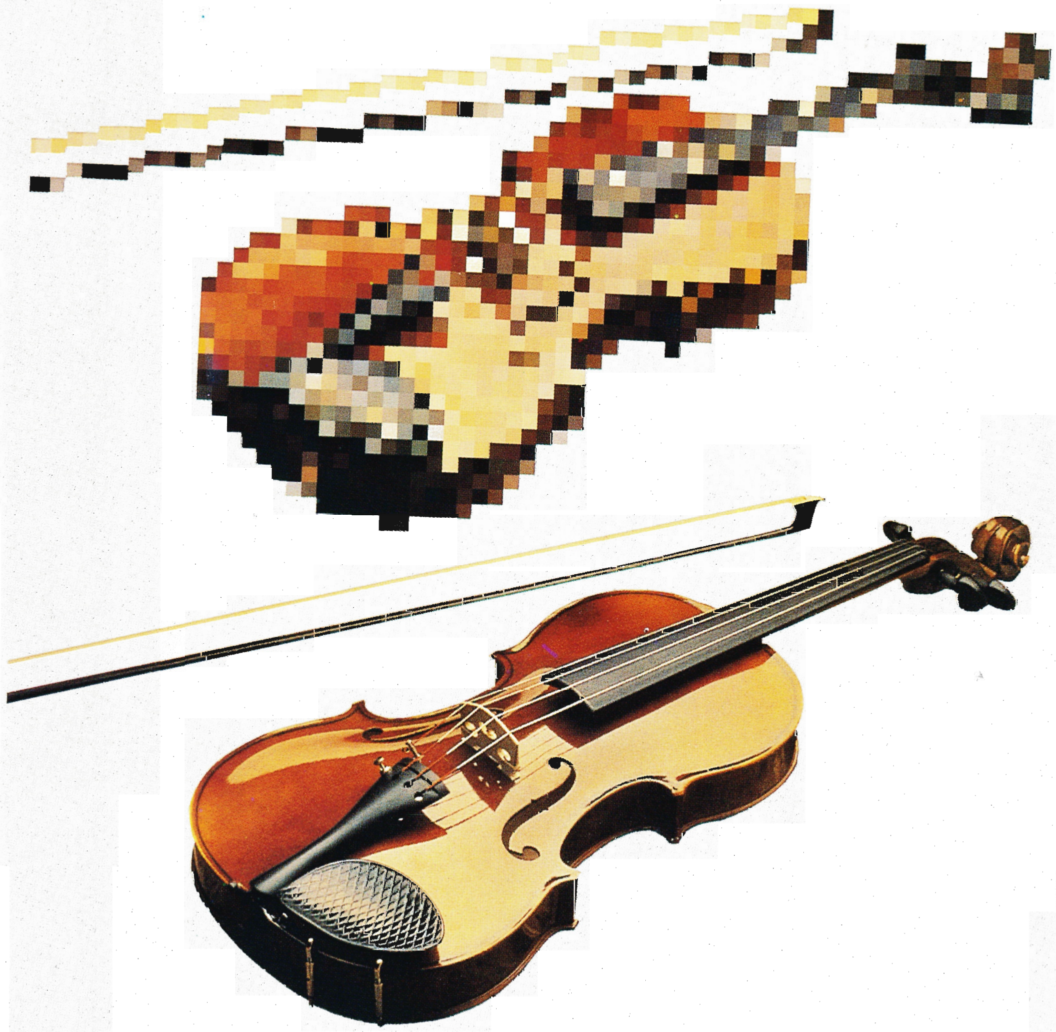
BITSTREAM CONVERSION



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Philips Components

PHILIPS

PHILIPS BITSTREAM CONVERSION

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Philips Bitstream A/D D/A Conversion

Background -

*Philips Bitstream Conversion is the technique of converting binary samples (eg. 16 bit words) into an one-bit code representing two levels ('0' and '1'), using Oversampling, Noise-shaping and Pulse Density Modulation (PDM). The **Bitstream** thus created is converted into an analogue signal using a switched capacitor bit-converter circuit. The very first Bitstream D/A converter for digital audio application was introduced by Philips Components in 1987, type No.SAA7320.*

There are other variations of this concept in use today. For example MASH (Multi Stage Noise Shaping) is a patented technique developed by Nippon Telephone and Telegraph (NTT) of Japan. MASH and other similar concepts convert the binary data samples into a data stream representing more than two levels (eg. 7 - 16 levels) by Oversampling, Noise-shaping and Pulse Width Modulation (PWM) [also referred to as Pulse Edge Modulation (PEM) or Pulse Length Modulation (PLM)]. The data stream thus created is converted into an analogue signal using a low pass filter.

Having recognized the major benefits, the digital audio industry is now adopting A/D, D/A conversion techniques based on these new concepts, which is revolutionizing the digital audio market. The software industry is also following this new trend with the release of Compact Discs recorded using Bitstream A/D conversion techniques. Audio critics of hardware and software alike are unanimously applauding the improvements in sound quality as a result of this new trend.

Recognitions -

*Following awards were presented to Philips in recognition of the development of the **Philips Bitstream PDM Conversion** technique:*

1. *Technology Award 1989*
   by Radio Gijitsu Magazine.
   Tokyo, Japan.

2. *Design and Engineering Exhibition*
   by 'The 1989 International Summer Consumer Electronic Show' committee.
   Chicago, USA.

Contents

EVOLUTION OF BITSTREAM (1-BIT) A/D/A CONVERSION

The concepts of Delta modulation and Sigma Delta modulation developed in the 1940's and 50's have been utilized primarily for voice transmission in telephony applications *(See reference 1, one of the first publications).* The emergence of advanced VLSI technologies (enabling powerful signal processing), and the development of new circuit techniques, have enabled the Sigma Delta concept to be adopted for high performance applications, like the Bitstream Conversion concept used in digital audio applications. These recent developments have demonstrated that the benefits of the new A/D and D/A conversion techniques based on Sigma Delta (1-bit) concept supersede the conventional PCM sample conversion.

The basis of the 1-bit technique is to exchange the **resolution in amplitude** with **resolution in time.** Information in the bitstream is represented by a highly oversampled 1-bit code. This article discusses Pulse Code, Delta, and Sigma Delta coding techniques.

Pulse Code Modulation (PCM)

In Pulse Code Modulation the amplitude of a signal is sampled with $F_s > 2 \times B_w$ (bandwidth) and quantized into discrete steps. The maximum signal amplitude defines the maximum quantizer range. Quantization error due to discrete steps cannot be removed from the signal. It results in white noise which spreads itself over the band until $f_s/2$ (see Fig.1). This results in the well known equation for dynamic range :

$$\text{Dynamic Range(dB)} = 6.02\text{dB} \times n + 1.76\text{dB}$$ (n= Number of bits)

If quantization is done at a higher sample rate, $N \times F_s$ (oversampling factor=N), error will spread itself up to $N \times F_s/2$ and noise contribution in the audio band will be reduced by 3 dB per factor 2 oversampling. In CD, quantization to 16 bits takes place at F_s in the studio and the dynamic range is therefore limited to 98 dB. In D/A conversion, this quantization noise cannot be removed from the signal by digital oversampling filters, with D/A converters of more than 16 bits, or by any other means.

Differential PCM / Delta Modulation

Differential Pulse Code Modulation (DPCM) is based on the idea of quantizing the derivative of the signal; i.e. when changes of the signal between sampling are small, the range of the quantizer can be reduced. With very high oversampling, the change of the signal during a sample period is reduced, thereby enabling the quantizer to be reduced to a 1-bit. Such a 1-bit DPCM coder is called a Delta Modulator (DM).

Fig. 2a shows the functional block schematic of a Delta Modulation stage. The input analog signal (a_i) is compared to the integrated output pulses (a_o) in the comparator and the difference signal (a_d) is fed into the coder (quantizer). In the coder, a positive pulse is generated when the difference signal a_d is negative and a negative pulse is generated when a_d is positive. If the difference signal is zero (eg. no input or DC), alternate positive and negative pulses are generated. The rate at which these pulses are generated is the sampling frequency of the signal. The signal consists of $\pm\delta$ pulses where δ is a single pulse.

Delta D/A:

Re-converting a delta modulated signal back into an analog signal requires an integrator (I) and a low pass filter (LPF) as shown in Fig. 2b. The integration of 1-bit pulses ($\pm\ \delta$) using a long time constant (compared to the sample period) integrator will yield a step waveform. Low pass filtering of the integrator output will generate an analog waveform which represents the original signal.

The quantization noise of a delta modulator is white at the output of the integrator. As in PCM coders, oversampling improves quantization noise in the audio band by 3 dB per factor 2 oversampling. The main difference between PCM coding and DM coding is that the maximum range of quantizer in DM is reduced to $\pm$ delta 'δ'. This is because the DM codes the differences in the signal amplitude and not the signal amplitudes on their own.

The dynamic range of DM can be improved by making the delta smaller, thereby generating less quantization error. The limit to which the delta can be reduced is given by the maximum derivative of the signal.

Assuming a signal of : $A_m\ \mathrm{SIN}(2\pi ft)$

the derivative is : $|\ 2\pi f\ A_m\ \mathrm{COS}(2\pi ft)\ | < \text{delta} / T$

(Where T=sample period, A_m = Maximum signal amplitude, f=signal freq.)

Exceeding this limit causes very strong distortion (slope overload distortion). Therefore the maximum derivative occurs at maximum signal frequency f_m and maximum signal amplitude A_m. If f_m is 20 kHz and A_m is full scale, this means that 'δ' has to be fairly high, resulting in high quantization noise level. Since speech and music usually have lower spectral energy at high frequencies, the 'δ' can be reduced further because f_m and A_m don't occur together. To design a good DM, assumptions about the signal spectrum have to be made. If these assumptions are not met, very strong slope overload distortion will occur.

Performance:

The main drawback of DM is the dependance of the dynamic range on the signal spectrum. Good dynamic range can be achieved only with a signal which has lowpass characteristics. Another drawback of single integration DM is the presence of correlated patterns at low signal levels.

Sigma Delta Modulation:

To overcome the slope overload problems of DM, Sigma Delta Modulation (SDM) was introduced. Similar to PCM, it quantizes the signal directly and not the derivative of the signal as in DM coding. This means that the maximum quantizer range is given by the maximum signal amplitude, independent of the frequencies in the band spectrum. Therefore no assumptions on the signal spectrum have to be made. Using a very high oversampling rate, the quantizer output can be reduced to a 1-bit.

The functional block diagram shown in Fig. 3a is a 1st order (single integration) SDM. The input of the quantizer is the integral of the difference between input and quantized output. This integrator forms a lowpass on the difference signal and ensures a good low frequency feedback around the quantizer. This feedback results in a reduction of quantization noise at low frequencies. Unlike in PCM and DM, the quantization noise of the SDM output is not white, but is colored with a first order high-pass characteristic (noise-shaping). Decoding of the SDM signal requires only a lowpass to remove strong high frequency quantization noise; i.e. to average the 1-bit code (see Fig. 3b).

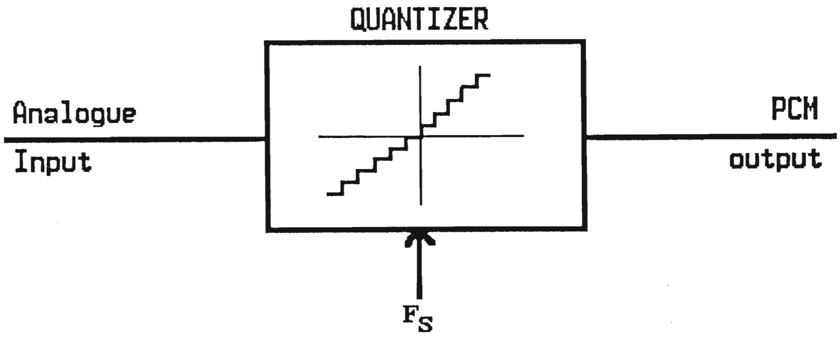
In a 1st order SDM, the quantization noise is highly correlated. Also, very high oversampling is required to achieve high resolution (256 x f_s for 12 bit). More effective noise-shaping can be achieved with multiple integration (higher order) SDM coders. But, coders with orders higher than 2 are potentially unstable and need special techniques like clipping to ensure stability. Architectures using several 1st or 2nd order coders (eg.MASH) can achieve higher order noise-shaping without stability problems, but rely on gain matching between the stages in the case of A/D. These cannot directly produce a 1-bit code, instead a multibit code of 3 or 4 bits is generated. Only the use of a 1-bit code for conversion can ensure high linearity at all signal levels independent of circuit element accuracies.

Future Trend:

The Digital Audio Market is increasingly adopting A/D D/A conversion techniques based on the Sigma Delta principle. The introduction of the D/A conversion device SAA7320 using the **Bitstream Conversion** concept, by Philips in 1987, has revolutionized the digital audio market. New A/D D/A conversion devices based on Oversampling and Noise-shaping (similar to Bitstream Conversion) are being introduced by major component manufacturers. Rapid improvements in A/D, D/A conversion performance and reduction in system cost can be expected due to the new concept.

Reference 1: DELTA MODULATION, A METHOD OF P.C.M. TRANSMISSION USING THE 1-UNIT CODE
by F. de Jager

Philips Res. Rep. 1,442-466, 1952.



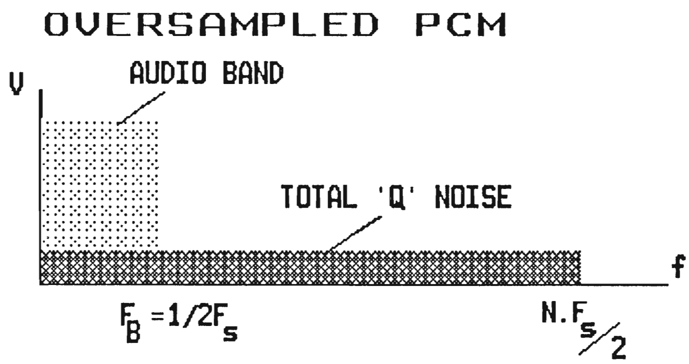


Fig.1 Pulse Code Modulation (PCM)

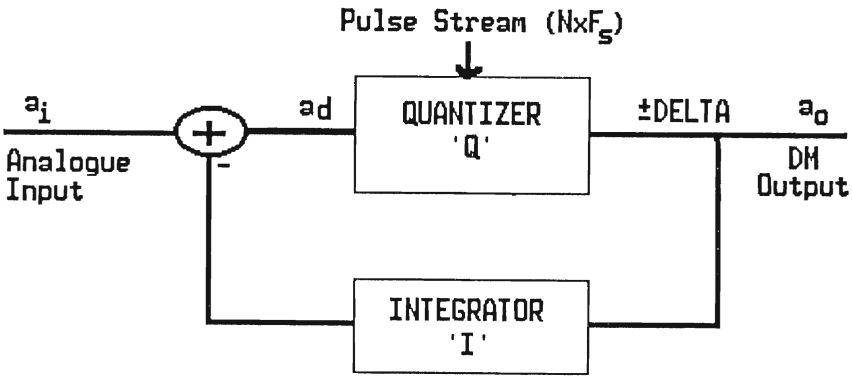


Fig.2a DELTA MODULATION (DM)

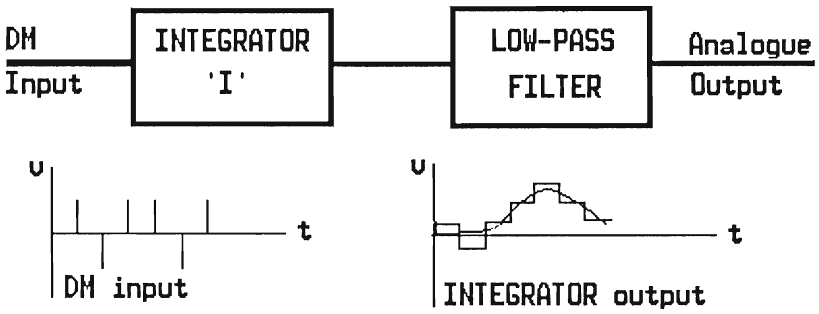
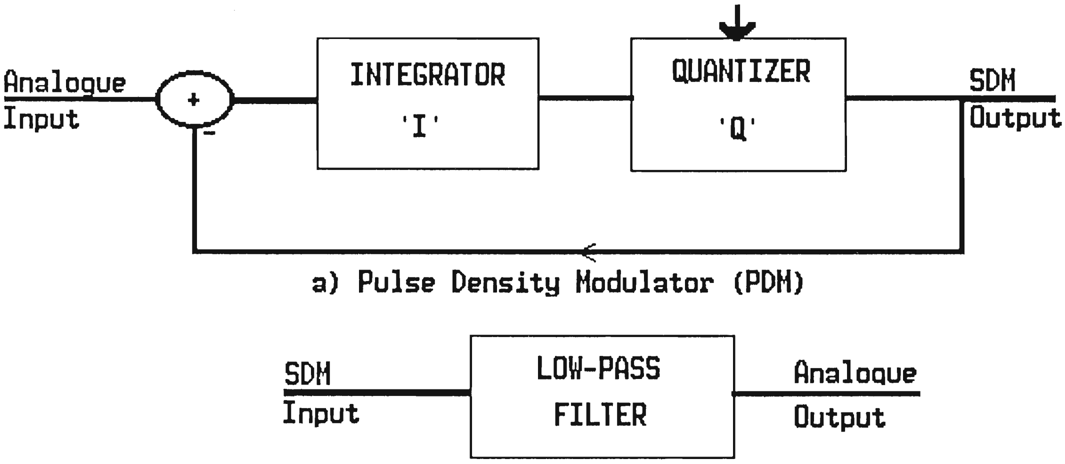


Fig.2b DM to Analogue conversion



a) Pulse Density Modulator (PDM)

b) SDM signal to Analogue

Fig 3. Sigma Dlta A/D, D/A conversion

INTRODUCTION TO BITSTREAM A/D,D/A CONVERSION

The steady growth of the digital audio market is making greater demands on both the equipment and the component manufacturers alike. The industry is continuously striving to further integrate functions on one hand and improve sound quality on the other. These efforts call for exploiting new technology and adopting completely new techniques. This report introduces the Bitstream A/D, D/A Conversion technique developed by Philips to meet these demands. The Bitstream Conversion technique greatly minimizes the influence of circuit inaccuracies on conversion resolution and linearity. Bitstream A/D, D/A Conversion can be implemented in CMOS technology, operating on single 5v supply. Inherent in the new concept is the ability to further improve audio performance while providing the means for total integration with other system functions on a single chip.

INTRODUCTION

The primary aim of any A/D, D/A conversion process should be to achieve good resolution and linearity in order to safeguard original waveforms. Non-linearity in A/D, D/A conversion introduces harmonic distortion. It is important not to introduce group delay differences which influence focus and stability of the sound sources in a stereo image. Performance at low signal levels and at higher frequencies is vital for good sound quality even though most specifications tend to focus on 0db and 1 KHz.

In conventional multibit A/D conversion techniques such as the successive approximation method, a multibit binary sample is directly generated from a sample and hold analogue value. In conventional D/A conversion techniques such as the binary weighted current divider method, an analogue current value is directly generated from a multibit binary sample value. These techniques rely heavily on the accuracies of the circuit elements, which are mainly analog. For example, a good 16 bit D/A converter has to generate a current value for the most significant bit (MSB) with an accuracy greater than 1/65,536 of the least significant bit (LSB). There are different techniques utilized to reach higher accuracies. Some of these methods are laser trimming of components for accuracy, segmentation of divider networks, Dynamic Element Matching (Philips patent) and simply adjusting the MSB and/or LSB currents by means of external trim pots. Any external adjustments which have to be performed on every device are liable to deteriorate due to aging and temperature.

In theory, any converter having more than a single bit is prone to non-linearity due to weighting errors on the binary code. This new technique developed by Philips performs most of the conversion process in the digital domain and avoids inaccuracies in the analogue domain. The conversion itself is performed on a 1-bit high speed data stream minimizing nonlinearities due to component mismatch.

A/D CONVERSION

The use of a steep anti-aliasing filter (>90 db) is of greater importance in A/D conversion (ADC) than in D/A conversion. This is because during A/D conversion aliasing components fall in-band rather than out-of-band as during D/A conversion (except by mixing). This demand on pre-filtering to reduce aliasing can be relaxed by using a higher sampling rate and digital filtering. In conventional multibit A/D conversion, the use of higher sample rates is limited by the speed of the DAC required in successive approximation (sample rate = No. of bits [16] x FS [44.1KHZ} x oversampling [2]). In the Bitstream Conversion technique it is possible to use higher sampling rates (64Fs and higher), hence any pre-filtering required will be simplified to mere first or second order.

A/D Building Blocks

Figure 1 A and B show the main functions in conventional successive approximation A/D conversion with and without the use of oversampling. Figure 1 C shows the main functions required in the Philips Bitstream PDM Conversion technique. The sampling rate used in this practical example is 64xFs (Fs is the final multibit sample frequency at the output of the ADC). A sample and hold function is not required because an input sample can be taken during every internal clock cycle, using a switched capacitor circuit. In successive approximation the sampled analog value has to be held for over B internal clock cycles. (B = No. of bits in a sample, e.g. 16)

(a) Low Pass Filter [LPF]

This is a second order analogue LPF with approximate phase linearity in the pass band.

(b) Analogue to Digital Converter [ADC]

A bitstream is generated from the low pass filtered analog signal by means of sigma delta modulation (SDM). Fig 2 shows the SDM stage where the feedback loop consists of:

- subtraction of output from the input to determine the approximation error

- loopfilter to extract the low frequency content of the approximation error

- quantizer to generate the best low frequency approximation for the next input sample

- a 1-bit DAC to convert the 1-bit output code into an analog signal to be compared with the input analog signal

Figure 3 shows a simulated pulse train from the quantizer in a third order SDM. For the purpose of illustration the input signal is shown at a reduced sample rate. Figure 4 shows a practical example where the one-bit code contains mainly high frequency noise above the base band. Fig. 5 shows the same signal in the frequency domain. It can be seen that the low frequency part of the quantization noise is very small and that the signal is coded with a high SNR in the base band. The feedback loop of the SDM shapes the white noise from the quantizer into a highly colored noise with minimal low frequency contribution (noise shaping). The high frequency noise is suppressed by the digital decimation filter behind the SDM.

(c) Decimation (down-sampling)

The decimation filter has two functions:

- Low pass filtering of the 1-bit code to produce the intermediate levels for the output pulse code modulation (PCM) word

- Band limiting the signal and the noise spectrum before sample rate reduction to Fs in order to minimize aliasing components

The decimation filter has two stages. When using a 64xFs input bitstream, the first stage of the filter calculates 192 multiplications of data and co-efficients to generate one multibit output sample. The output sample rate of the first stage is 2xFs. The second stage of the decimation filter uses a multibit multiplier with full convolution performed at the output sample rate of Fs. When using a finite impulse response (FIR) type filter, down-sampling can be simplified to calculating a sample every 1/Fs sec. as the filter is non-recursive. Figure 6 summarizes the main steps in Bitstream A/D Conversion and their frequency domain characteristics.

D/A CONVERSION

In the Bitstream D/A Conversion process the binary samples (16 bits) are converted into a high speed (e.g. 11 MHz) 1-bit data stream which is then converted into an analog signal using a 1-bit DAC. Using the digital domain to transform the weighting on bits in a binary sample into the 1-bit data stream eliminates the major source of non-linearity in D/A conversion.

D/A Building Blocks (e.g. Philips device numbers SAA7320, SAA7321)

Figure 8 shows the main functions in Philips PDM Bitstream D/A Conversion. They are: Digital filtering and oversampling; noise shaping and code conversion to generate a 1-bit data stream; and a 1-bit DAC to generate an analog signal from the 1-bit data stream.

(a) Digital Filtering and Oversampling (SAA7320, SAA7321)

The first of the three stages used for oversampling is conveniently utilized to attenuate the periodic images of the input signal by digital filtering (see Fig 9). A non-recursive FIR interpolation filter is best suited for higher performance applications as it is phase linear and has less overshoots and shorter settling time. First order noise shaping is done in the accumulator of the multiplier in the filter. Down scaling of the signal is implemented to prevent clipping during any overshoots. The gain of the filter is chosen to compensate for influences in-band due to other stages in the conversion path as shown in Fig 10. In the second stage, 32 times oversampling is performed by linear interpolation. In the third stage, two times oversampling is performed using sample and hold. Fig. 11 shows the oversampling steps that generate a final sample rate of 11.2896 MHz (256Fs).

An internally generated out-of-band dither signal of -20 dB at 352 KHz is introduced in the second stage of oversampling. This is in order to reduce any idling patterns from the noise shaper. To accommodate the dither signal one MSB is added. Therefore the output of the final oversampling stage is 17 bit samples at 11.2896 MHz.

(b) Noise Shaper and Quantizer (Unicoder)

When using noise shaping coders in combination with oversampling, word length of samples can be reduced. One-bit coding is an extreme example of code conversion. The quantization noise introduced by the reduction of wordlength is spectrally shaped by digital lowpass feedback around the quantizer, maintaining a good low frequency resolution.

Figure 12 shows the block diagram of the quantizer and noise shaper. The signals are in the 2's compliment format. The 1-bit code from the quantizer is the sign bit. The rest of the sample, referred to as the quantization error, is fedback after a limiter operation to prevent overflow. The second order noise shaping is done by adding double the error and the negative value of the error to the previous two samples as shown in Fig 12. Minimum of a 21 bit data bus is required to handle the data within the loop.

(c) Bitstream D/A Converter (Bit Converter)

The 1-bit data stream at 11.2896 MHz is converted into an analog signal using a switched capacitor network as shown in Fig 13. Two control signals representing logic '0' and '1' of the data stream together with a continuous clock, control the switching of the capacitors. During the negative half of the clock, capacitor C2 is charged and C1 is discharged. During the positive half, if the 1-bit data is a logic '1', the capacitor C1 is charged by taking a fixed amount of charge from the summing node of the op-amp. If the 1-bit data is a logic '0', a fixed amount of charge is transferred into the summing node from C2. Resistor R1 and capacitor C4 serve as the first section of a third order analog filter which is used to attenuate the HF quantization noise, the periodic images around 4 Fs and the dither frequency. Fig. 14 illustrates how the Bitstream D/A Conversion is able to regenerate analog waveforms closer to the original.

LINEARITY OF BIT STREAM CONVERSION

Linearity of Bitstream Conversion does not rely on matched elements. There are only + and - full scale reference points. Intermediate points are determined by time averaging. Any errors in the two reference values give only a gain offset error but not a linearity error. Figure 7 illustrates the effect on linearity due to element mismatch in 1-bit and multibit ADs and DAs.

Non-linearities in the Bitstream Conversion technique can originate from two possible sources. The first, at very low signal levels caused by idle patterns from the noise shaper/quantizer, can be minimized by the use of dither signals. The second, at high signal levels caused by the analog signal processing components (e.g. op-amps, capacitors), can be minimized by careful components selection.

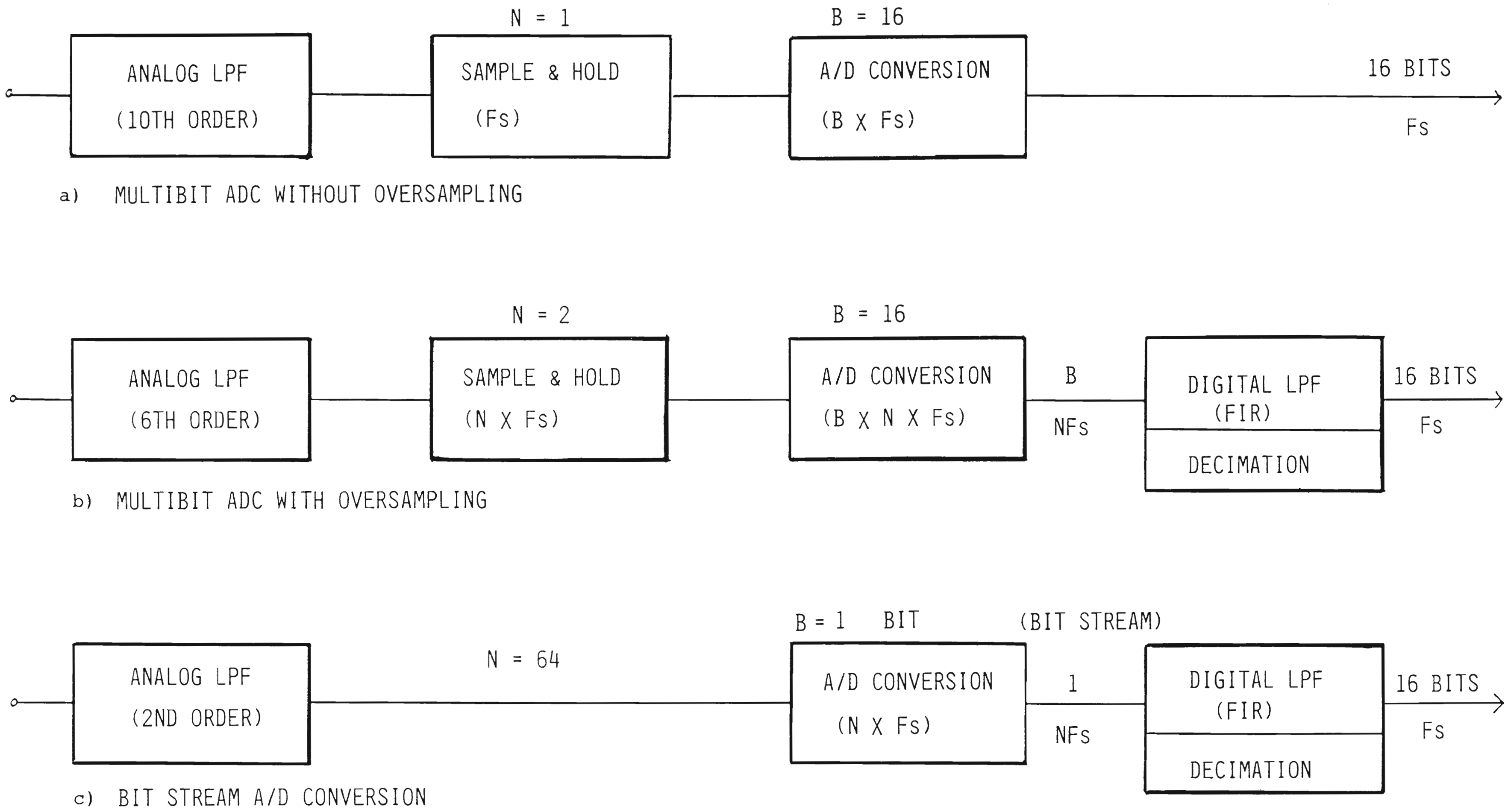
DISTORTION

The low level distortion in multibit DACs is caused by the MSB change around zero signal resulting in glitches and matching errors. In the one-bit converter there is no MSB change around zero because zero is represented by an equal number of positive and negative fullscale pulses. For a small signal the ratio of the positive and negative pulses is changed. The result is very low distortion at low signal levels.

CONCLUSION

Inherent in the Multibit A/D, D/A Conversion system is non-linearity due to mismatching of conversion elements. The Philips Bitstream Conversion technique overcomes this by using a 1-bit converter. The number of bits in a sample can be reduced to a single bit without losing resolution by means of oversampling and noise shaping.

The Philips Bitstream A/D, D/A Conversion technique can be implemented in standard CMOS technology. Inherent in the Philips Bitstream Conversion concept is the ability to achieve very high levels of sound quality. It is also well suited for total integration of A/D and D/A's with other system functions using VLSI technologies.



Fs - SAMPLING FREQ. N - OVERSAMPLING FACTOR B - NO. OF BITS/SAMPLES

FIG. 1 MULTIBIT AND BITSTREAM A/D CONVERSION

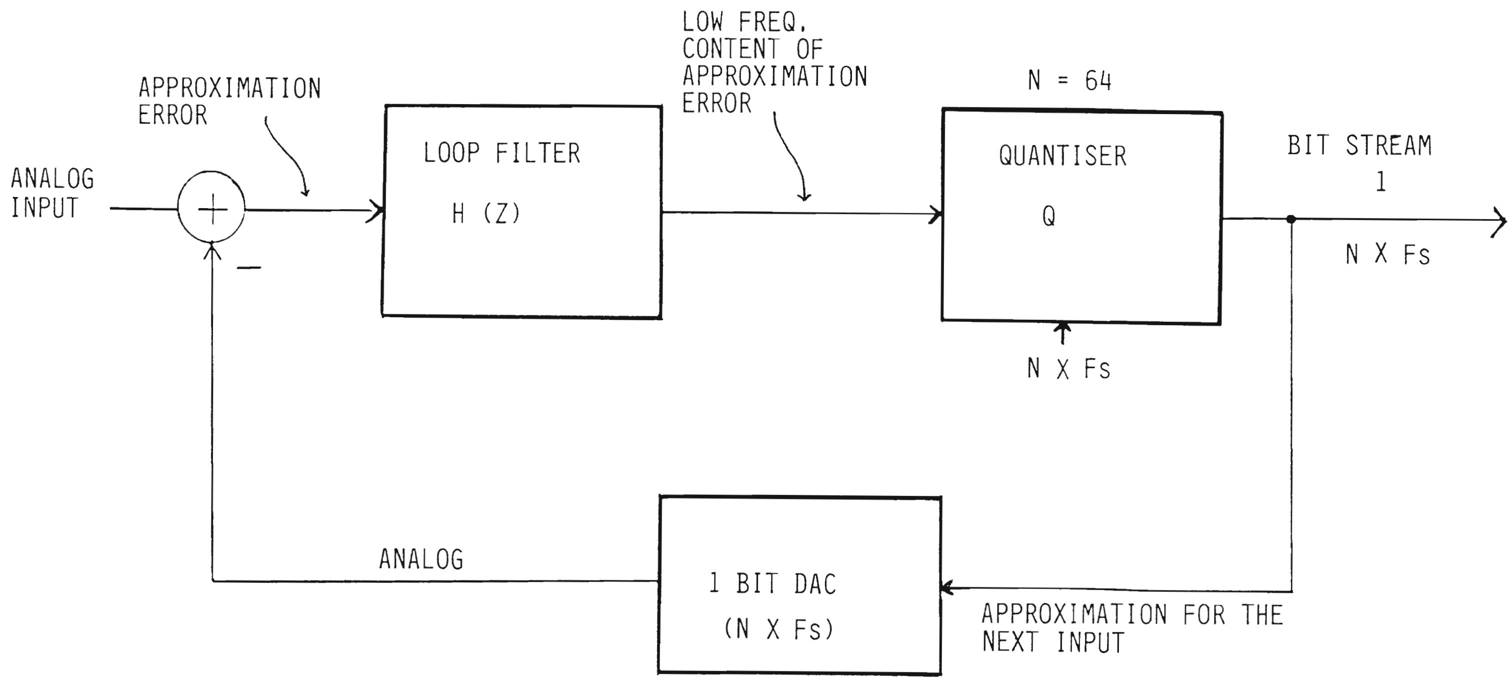


FIG. 2 BITSTREAM GENERATION BY
SIGMA DELTA '$\Sigma - \Delta$' MODULATION (SDM)

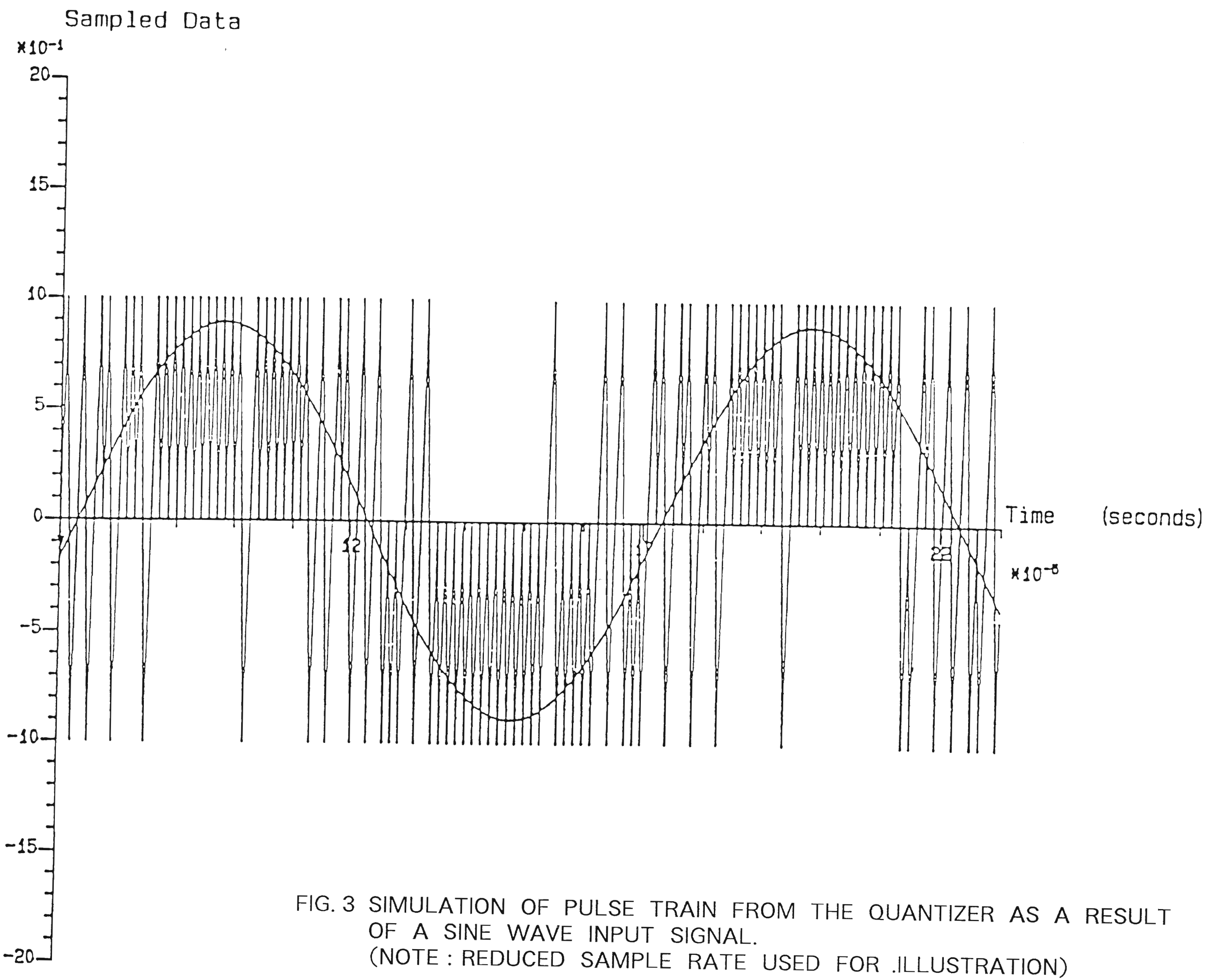


FIG. 3 SIMULATION OF PULSE TRAIN FROM THE QUANTIZER AS A RESULT OF A SINE WAVE INPUT SIGNAL.
(NOTE : REDUCED SAMPLE RATE USED FOR ILLUSTRATION)

FIG. 4 PRACTICAL EXAMPLE OF PUISE TRAIN (BITSTREAM) FROM QUANTISER DUE TO A SINE WAVE INPUT. (SIMULATED)

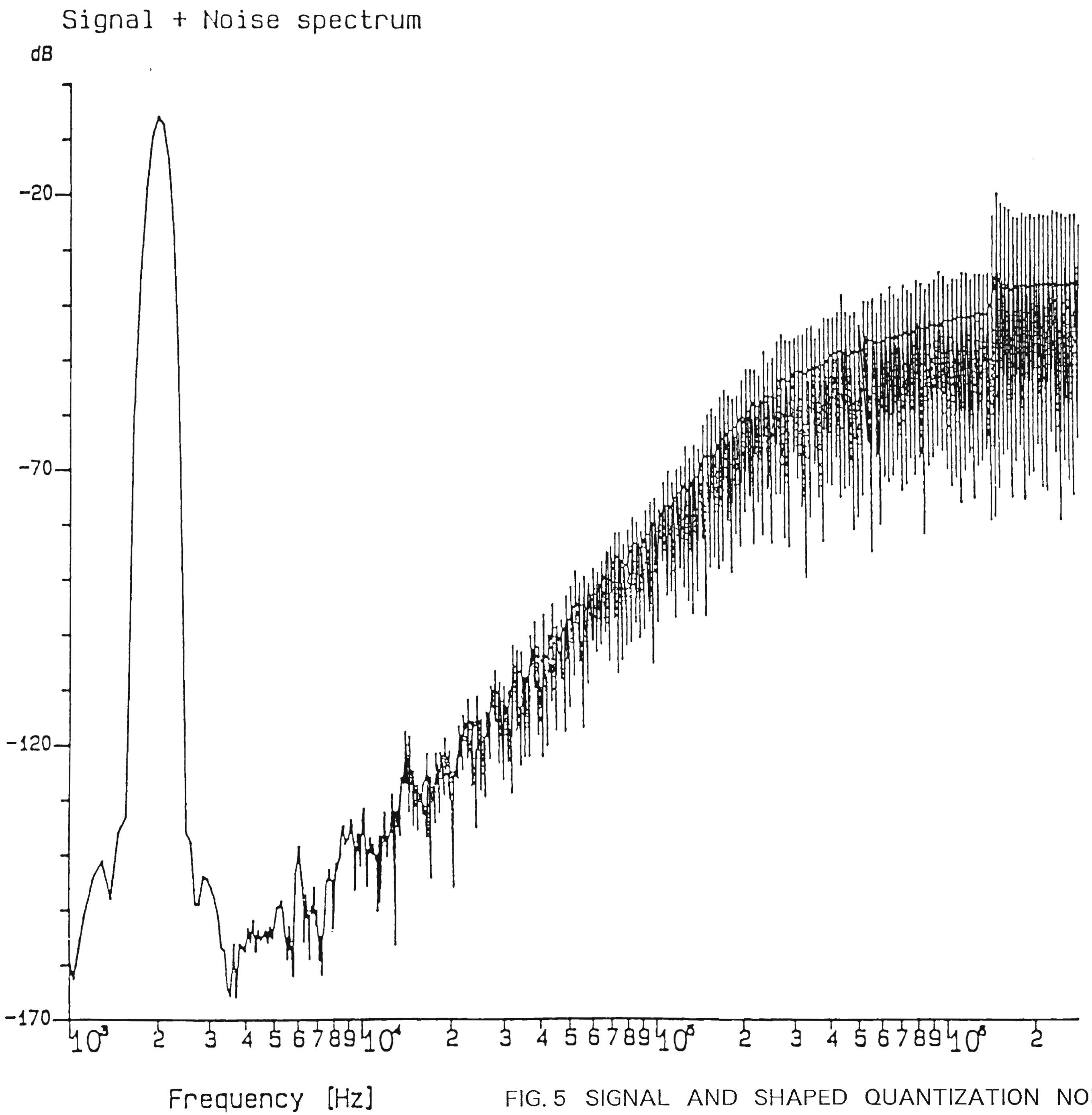
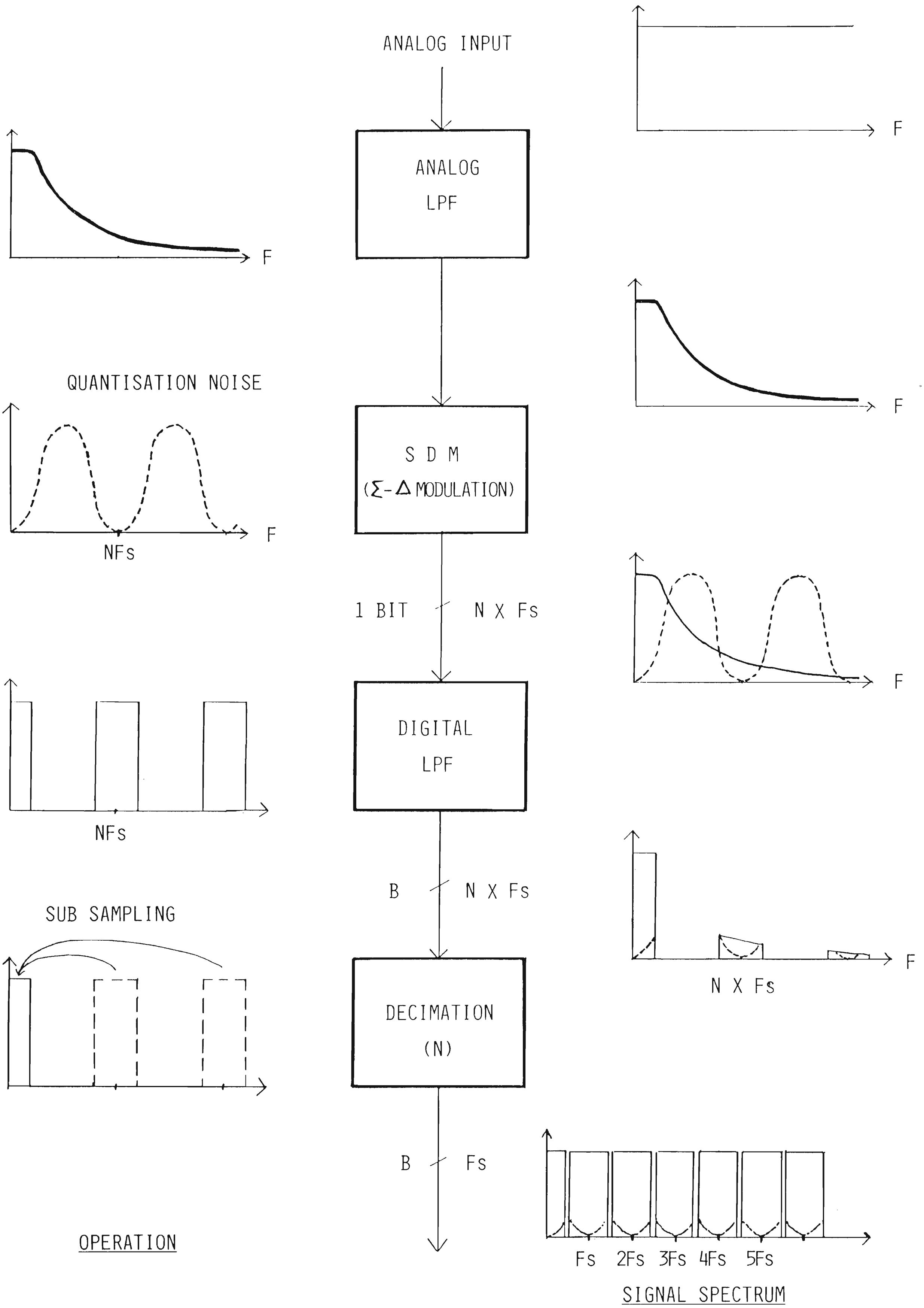


FIG. 5 SIGNAL AND SHAPED QUANTIZATION NOISE OF A 3RD ORDER SDM (FREQUENCY DOMAIN)



F_s — SAMPLING FREQ. Eg · 44.1KHz
B — NO. OF BIT／SAMPLE Eg · 16.
N — OVERSAMPLING FACTOR.

FIG. 6 SPECTRAL CHARACTERISTICS OF BITSTREAM A／D CONVERSION OPERATIONS (FREQUENCY DOMAIN)

FLOW DIAGRAM OF SAA7321 DATA PATH

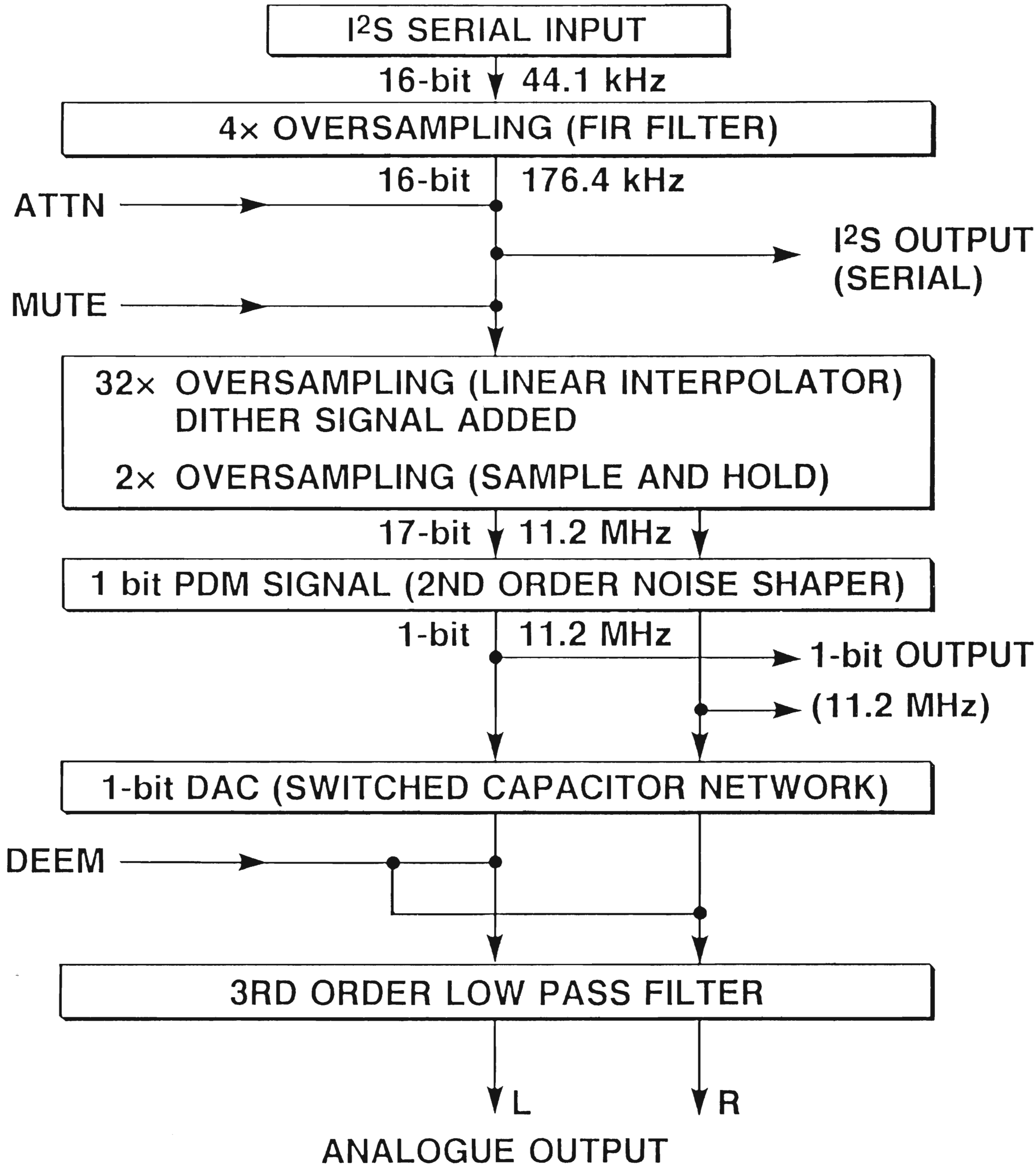


FIG. 7 MAIN FUNCTIONS IN BITSTREAM D/A CONVERSION

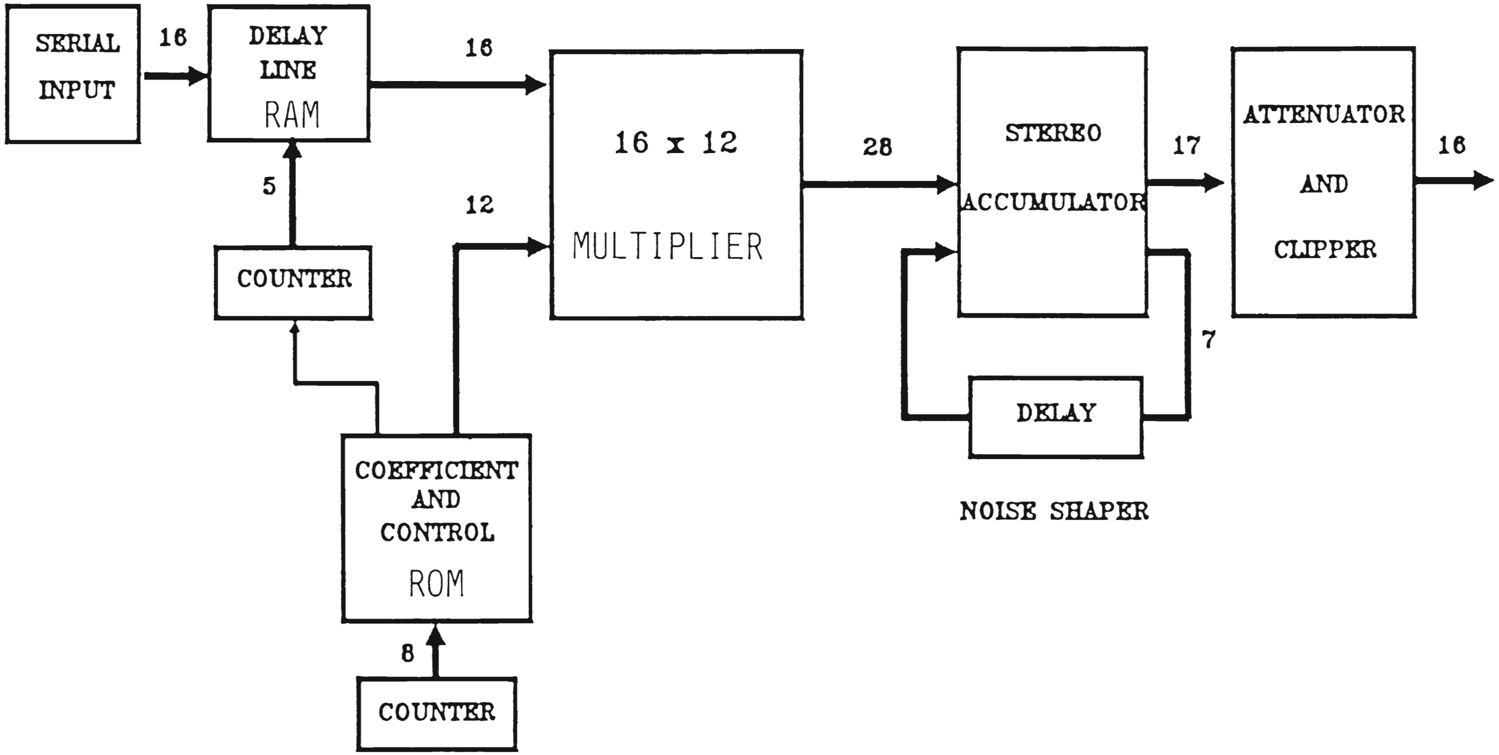


FIG. 8 $4F_s$ FIR DIGITAL FILTER WITH NOISE SHAPING (SAA 7320/7321)

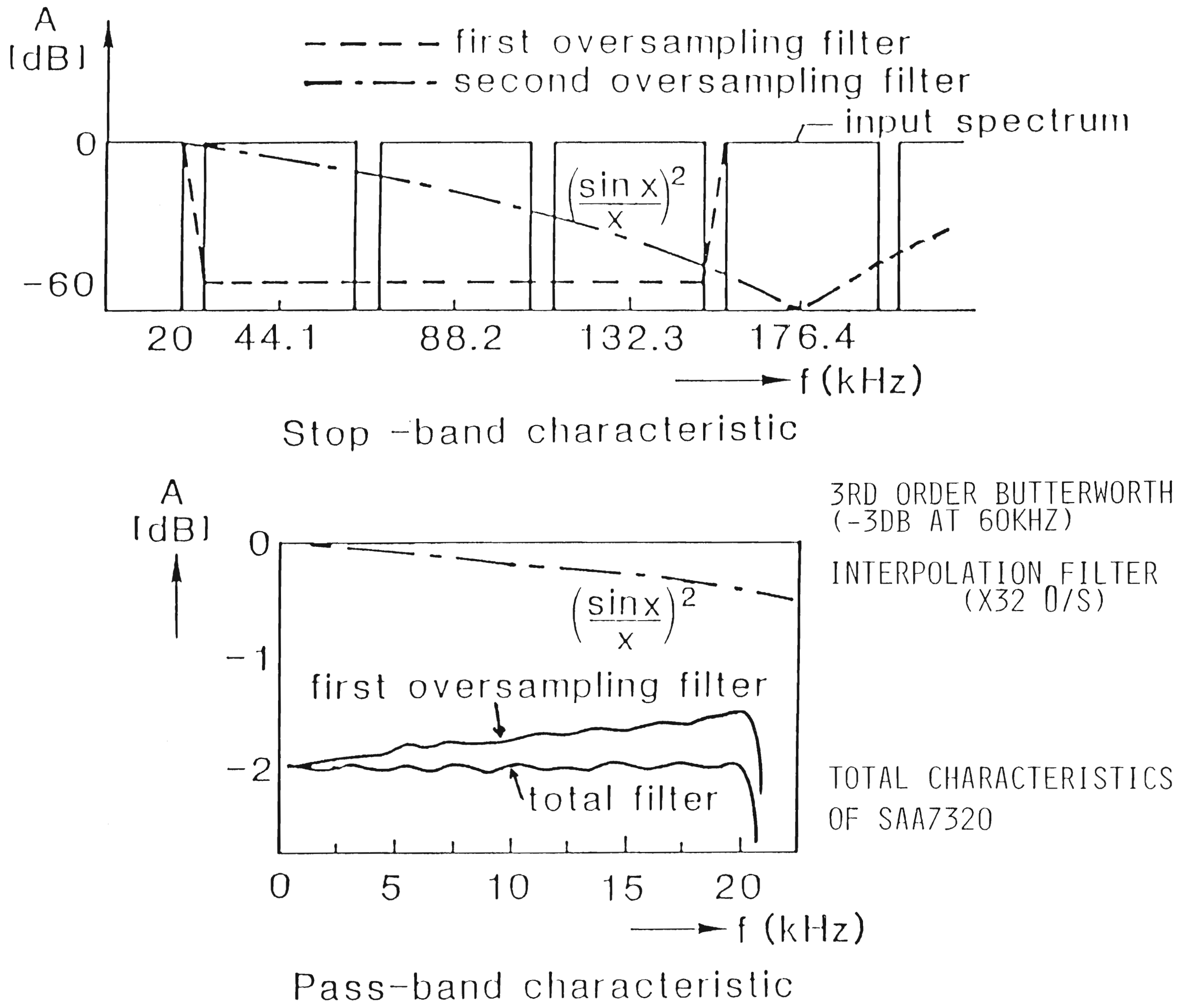
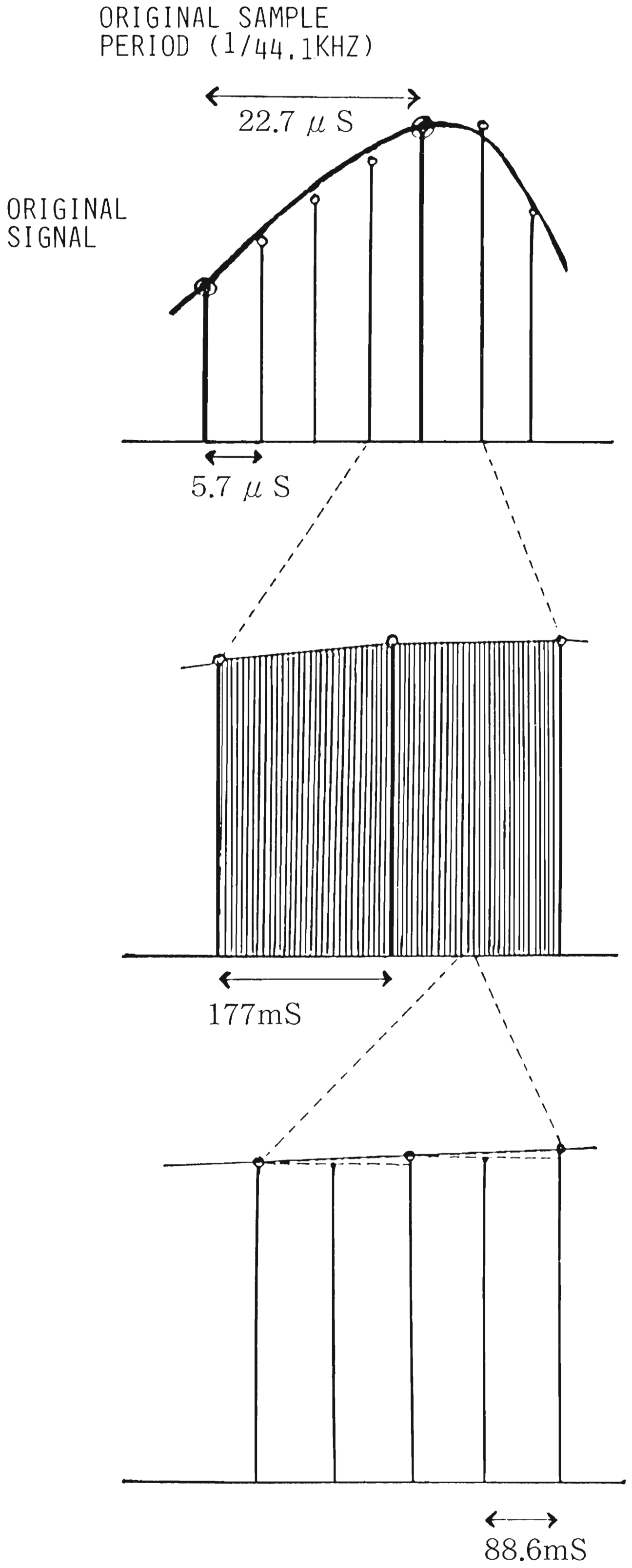


FIG. 9 FILTER CHARACTERISTICS OF OVERSAMPLING STAGES



<u>4 TIMES OVERSAMPLING</u>
(INCLUDE DIGITAL FILTERING)

<u>32 TIMES OVERSAMPLING</u>
<u>BY LINEAR INTERPOLATION</u>

FILTERING CHARACTERISTICS -

$$= \frac{\sin x}{x}, \quad \text{WHERE } x = \frac{2\pi F}{N\,Fs}$$

N = INTERPOLATION RATIO
Fs= INPUT SAMPLE FREQUENCY

<u>2 TIMES OVERSAMPLING</u>
<u>BY SAMPLE HOLD</u>

FINAL SAMPLE RATE -
= 4 x 32 x 2 = 256 x 44,100
= <u>11.2896 MHZ</u>

FIG. 10 OVERSAMPLING

NOISE SHAPER

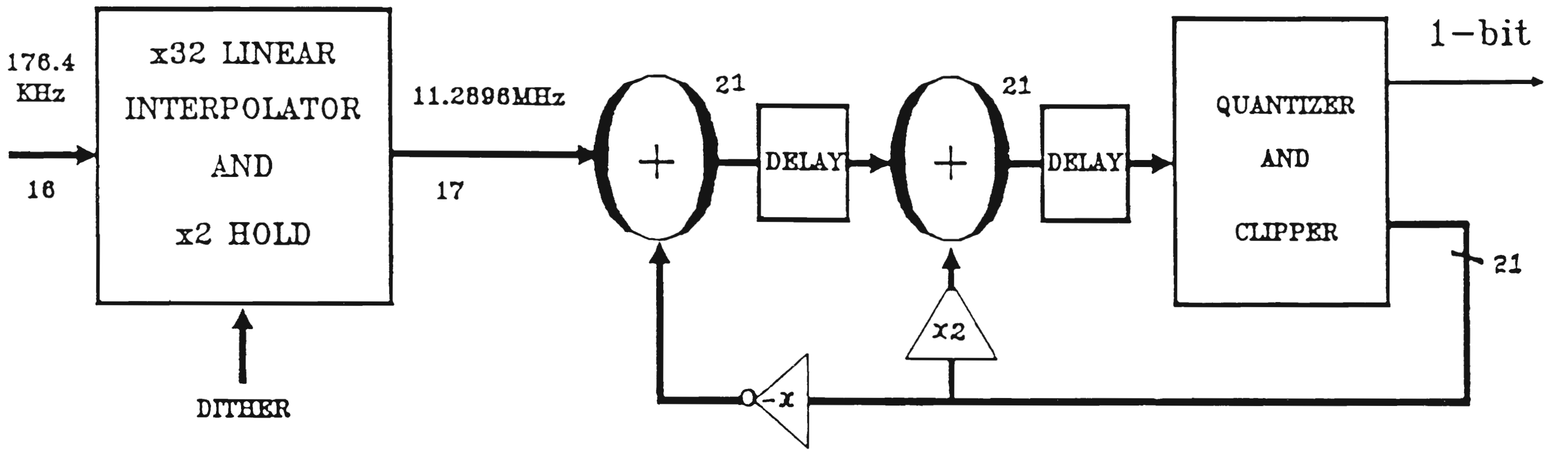


FIG. 11 NOISE SHAPER AND QUANTIZER

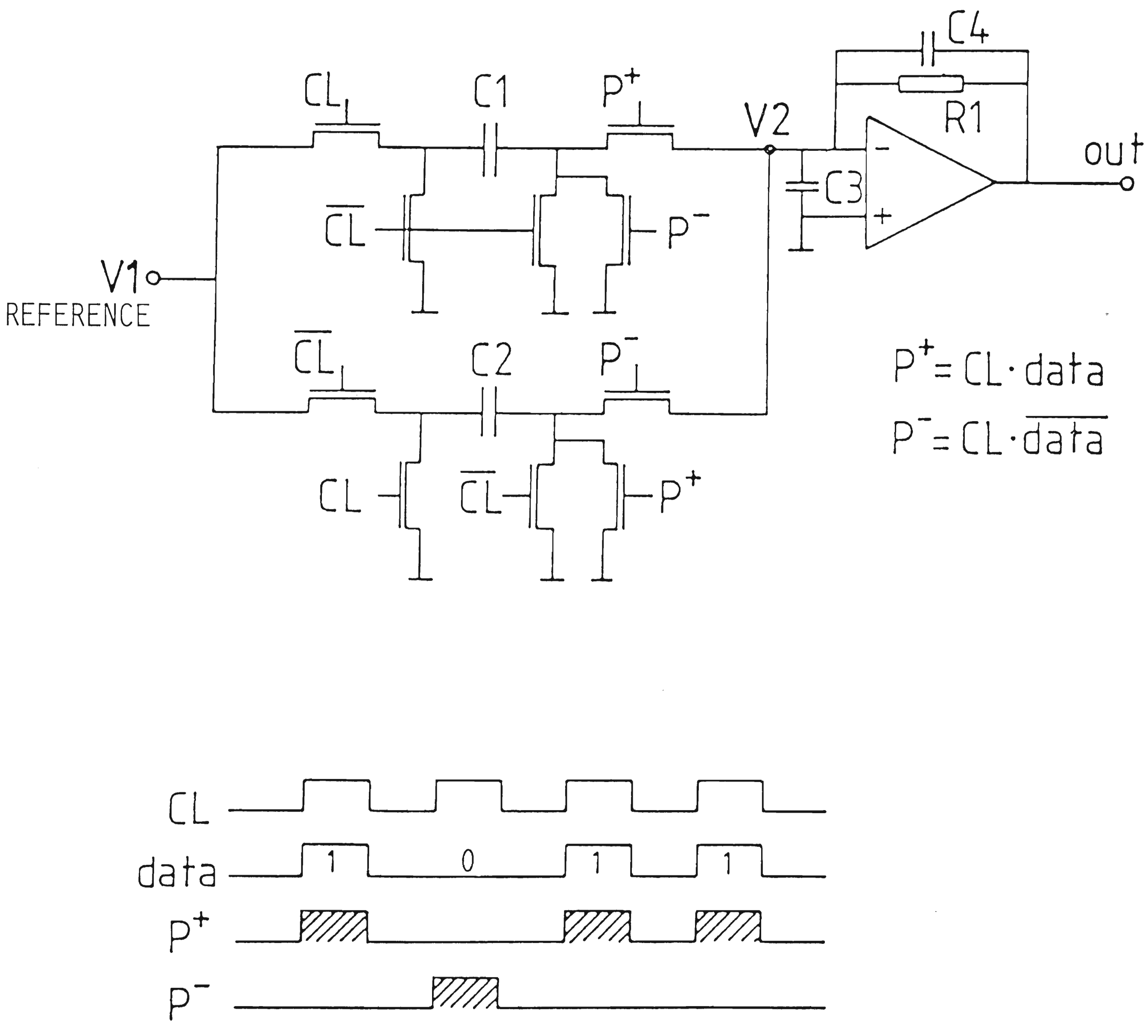


FIG.12 SWITCH CAPACITOR BIT-CONVERTER

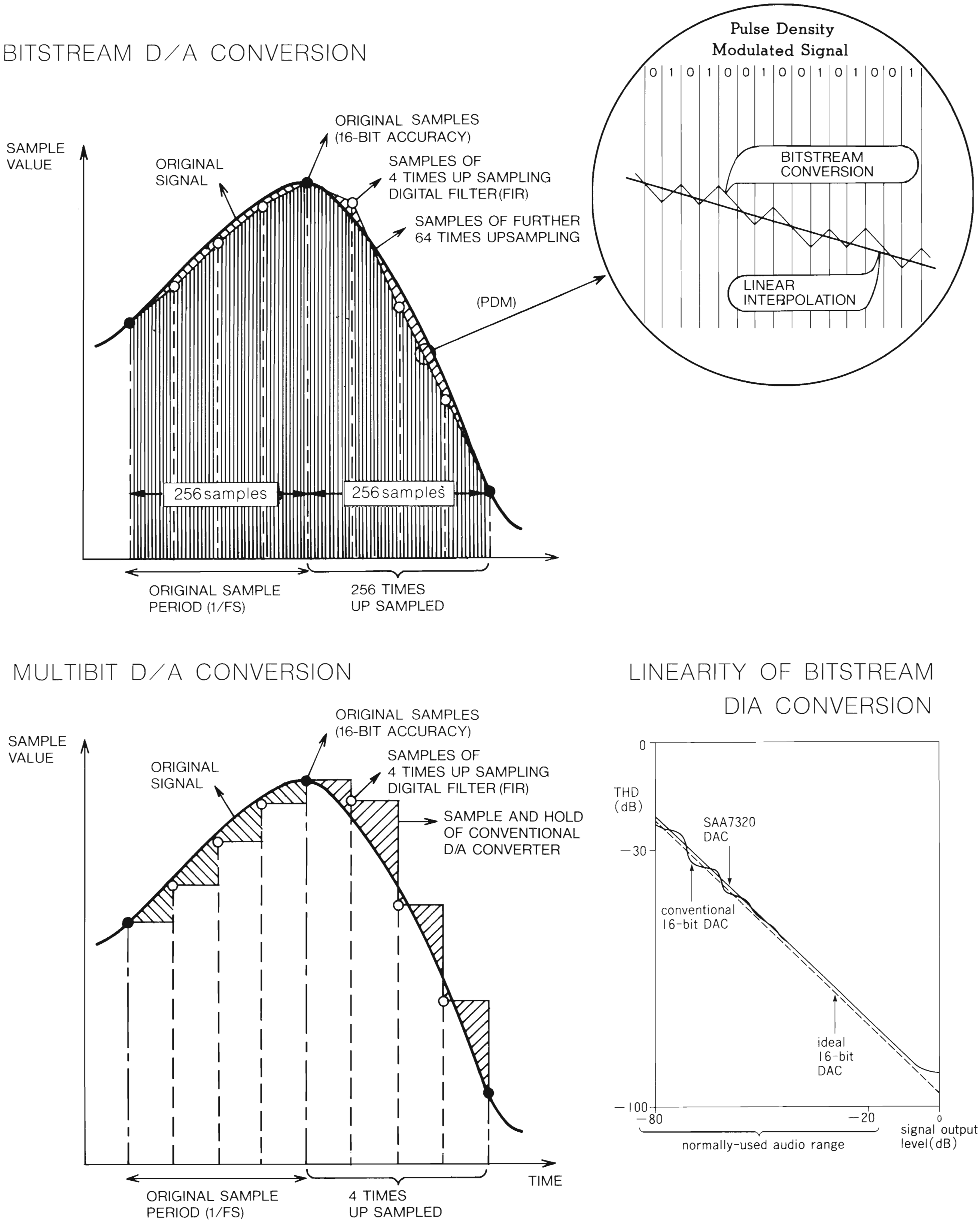
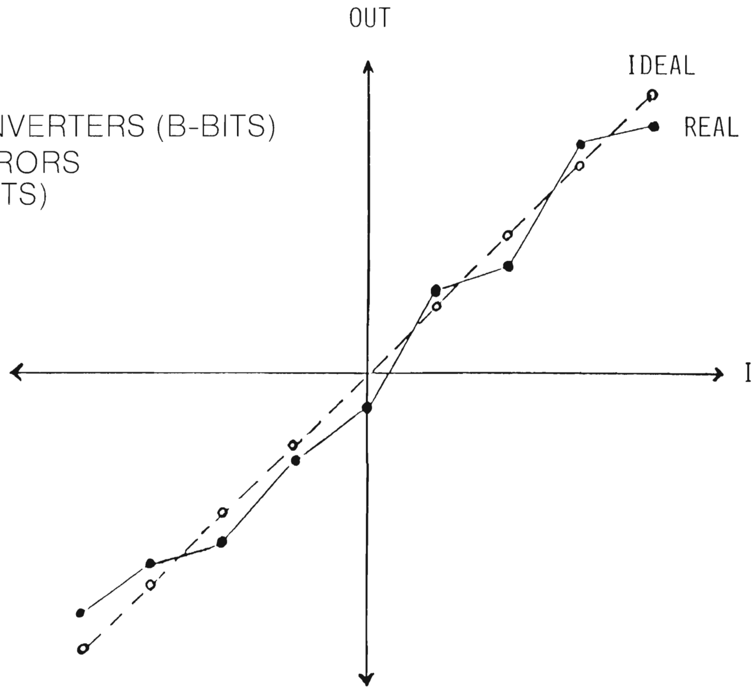


FIG.13 BITSTREAM AND MULTIBIT D/A CONVERSION

A. MULTIBIT CONVERTERS (B-BITS)
LINEARITY ERRORS
('B' REF, POINTS)



B. I-BIT CONVERTERS
GAIN ERROR
(TWO REF, POINTS ONLY)

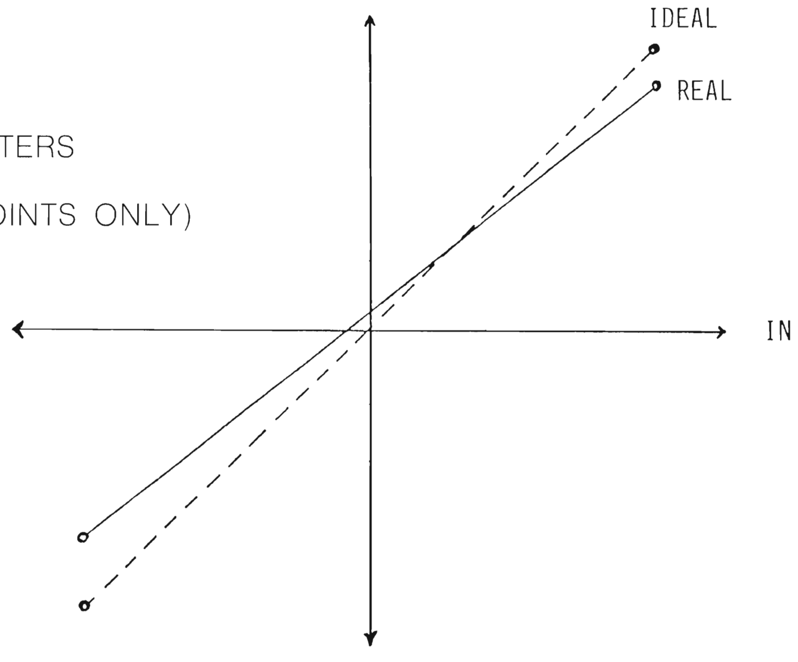


FIG.14 LINEARITY OF MULTIBIT AND BIT STREAM (1-BIT) A/D,D/A CONVERSION

OPERATION OF A 2nd ORDER NOISE-SHAPER AND AN UNICODER

Introduction:

The following is an introduction to the operation of a second order Noise-shaper circuit, similar to the ones used in Philips Bitstream PDM D/A Conversion systems. The circuit performs two functions: noise-shaping by means of feedback loops (integration): and, generation of a Bitstream code for conversion into an analogue signal.

A second order Noise-shaper consists of two integration loops (Loop Filters) for quantization error and a Unicoder for generating the bitstream. The structure looks different from a Sigma Delta Modulator (SDM), but performs the same 2nd order noise-shaping on the quantization error. The coding structure adopted in Bitstream Conversion is better suited for digital implementation than an SDM structure.

Operation of 2nd order Noise-shaper:

The operation of the Bitstream Noise-shaper and Unicoder, as shown in Fig. 1, is explained by indicating the values of the audio samples occurring in each of the stages during few sample periods (Table 1). When using 2nd order noise-shaping, Philips Bitstream conversion utilizes 256 times oversampling of the original signal (e.g. 44.1KHz sampling rate of Compact Disc), resulting in a sampling rate of 11.2896 MHz.

For the purpose of simplicity of explanation, the maximum value of a 16 bit sample (0 dB) is represented as unit value '1'. However, using a constant 0dB input will result in an infinite accumulation of errors, thus resulting in infinitely high values in the loop. In practice, to prevent this overload in the loop, the input has to be down-scaled in the digital filter by at least 1 dB. In the analysis of the operation of the noise-shaper shown in Table 1, the calculations are done by using a constant input of 0.5 (-6dB), generating an 1-bit output with an average of 0.5. Two arbitrary initial values are chosen for the contents of the two delay registers at time t_0 in order to show the operation (D = 0.5, G = -.6).

At t_0 the input is 0.5 representing a -6dB signal. The value of G being negative the 1-bit value of H in the bitstream is -1. Therefore I = 0.4, which also equal J, [{-0.6+(-)-1}]. Then E=2*J=0.8 and C=A-J=0.1 which will equal to D at time t_1. The value of F during time t_0 is equal to D+E=1.3 which will equal to G at time t_1. Table-1 continues to show the values occurring at the different stages of the noise-shaper at times intervals t_1, t_2, t_3, t_4. As the values inside the loops are much larger than the unit value '1' represented by 16 bits samples, the width of data busses in the loops need to be as wide as 22 bits or more to handle the signals without significant loss of performance.

The calculation shown in the Table-1 may be continued using a large input level to observe the need for a Limiter function to prevent overloading of the noise-shaping loops.

Unicoder:

The output of the Unicoder (quantizer) is a '+1' if its input is positive (MSB = 0), or '-1' if the input is negative (MSB = 1). In an adder, the quantization error 'I' is calculated by (G-H) and this error is fed back into the double integration loops. To prevent overflow in the loop at very high inputs (> -1dB), a limiter (clipper) function is utilized to limit the fed back quantization error J.

Idling :

Noise-shaper Coders have accumulation/delay in the feedback loops which determine the characteristics of noise-shaping. With no signal input, a coder ideally should generate a tone at 1/2 N f_s only, but due to noise-shaping characteristics, additional low level tones may be generated. In order to minimize these tones, AC and/or DC dither patterns can be added to the input signal so that the noise-shaper coder continues to operate with a changing signal even when the original input is zero or DC.

Other techniques:

Combination of independent 1st and 2nd order Noise-Shaper Coders (NSC) to form higher order noise-shaping is possible. The resulting coder (quantizer) in these architectures **is multibit** (Multicoder) **and not 1-bit** (Unicoder). The "MASH" concept developed by NTT of Japan and adopted by some component manufacturers, use multi stage noise-shaping. The circuit shown in Fig.2 is an example of a "MASH" noise-shaper coder as used in a D/A converter operating at 64 x Fs. It combines a 1st order 5 level NSC with a 2nd order 2 level NSC resulting in a 3rd order 7 level NSC. The 3 bit (7 level) output is converted into a Pulse Width Modulated Signal (PWM). The information in the 3 bit code is represented by the width of the pulse. Hence in PWM the timing of the pulse transition should be controlled accurately to achieve quality audio performance.

Further improvements in circuit techniques will enable higher orders of noise shaping at higher oversampling rates. In implementing such architectures the theoretical improvements possible should be verified with actual measured achievements.

TABLE 1

Noise Shaper Operation

	A	B	C	D	E	F	G	H	I	J
t0	0.5	-0.4	0.1	0.5	0.8	1.3	-0.6	-1	0.4	0.4
t1	0.5	-0.3	0.2	0.1	0.6	0.7	1.3	+1	0.3	0.3
t2	0.5	0.3	0.8	0.2	-0.6	-0.4	0.7	+1	-0.3	-0.3
t3	0.5	-0.6	-0.1	0.8	1.2	2.0	-0.4	-1	0.6	0.6
t4	0.5	-1.0	-0.5	-0.1	2.0	1.9	2.0	+1	1.0	1.0

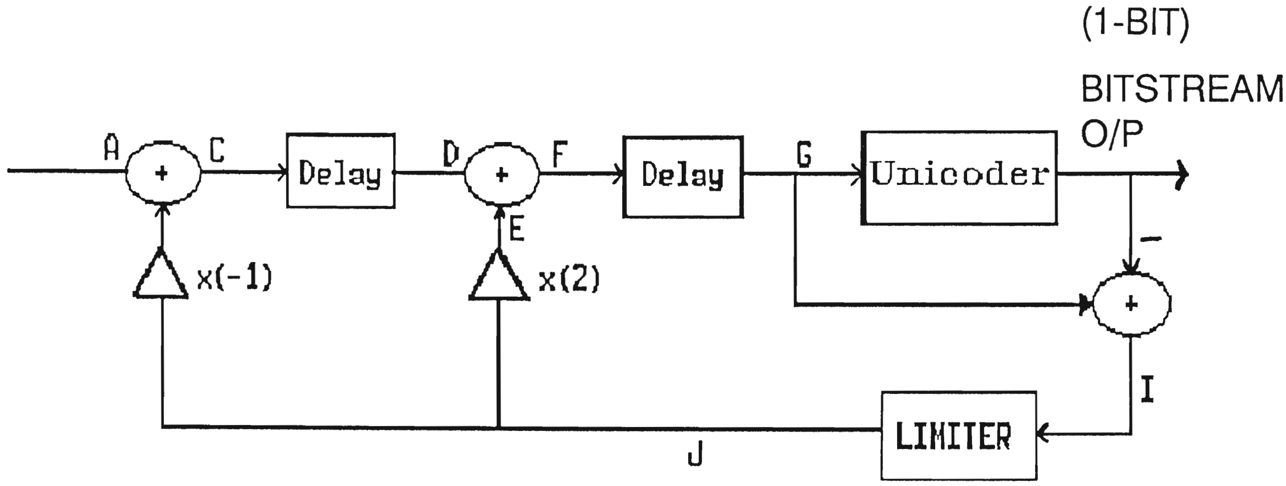


Fig.1 2ND ORDER NOISE-SHAPER AND UNICODER. (BITSTREAM D/A)

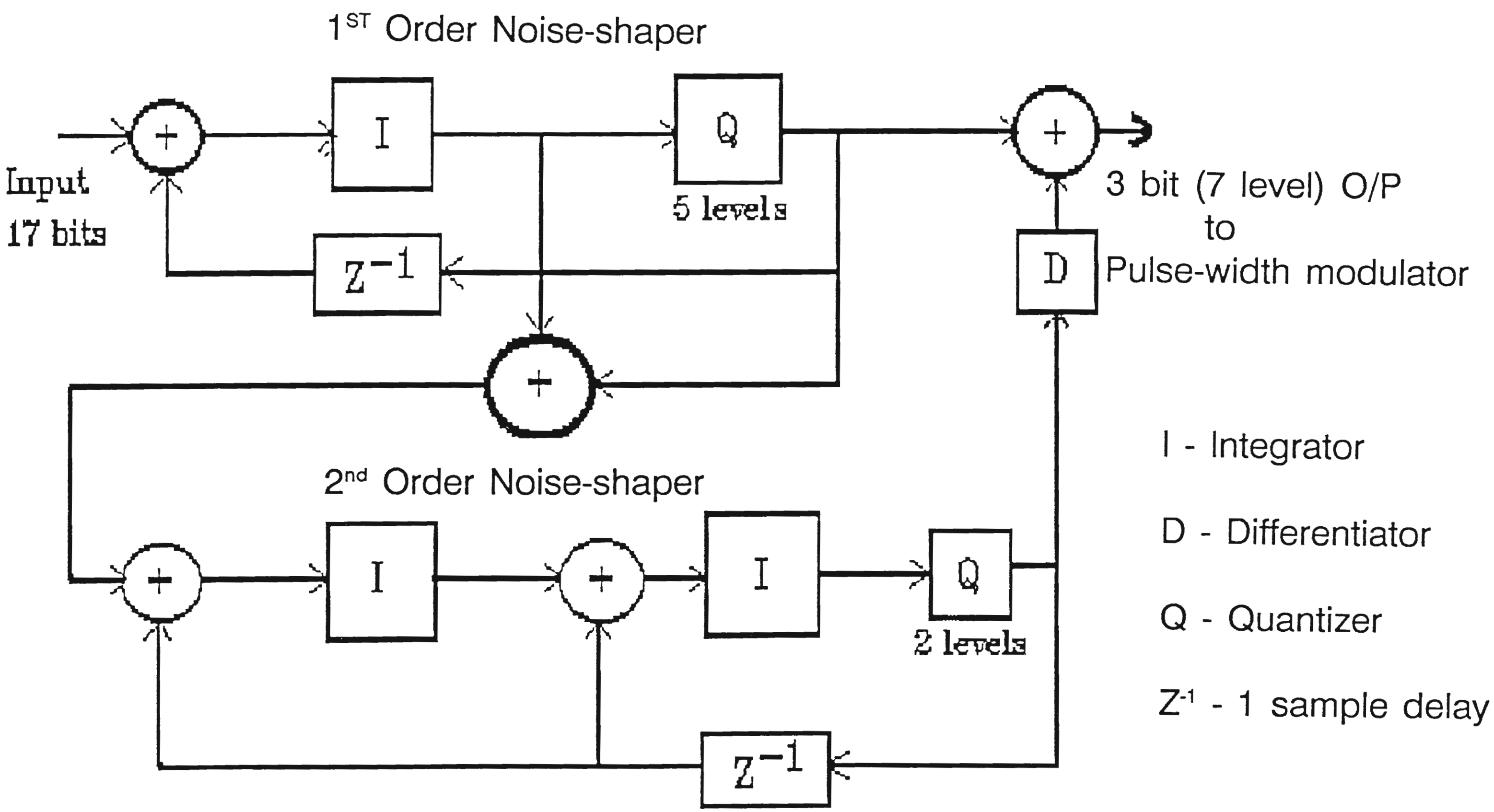


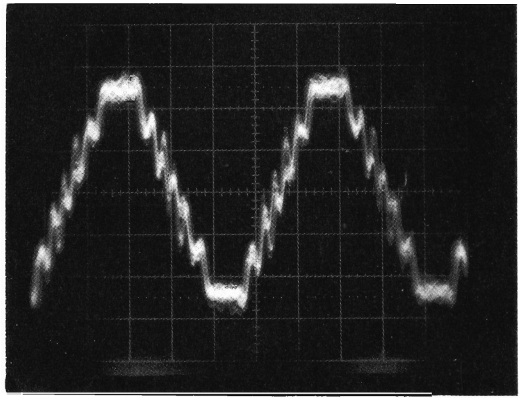
Fig.2 EXAMPLE OF MULTISTAGE NOISE-SHAPER (as in MASH).

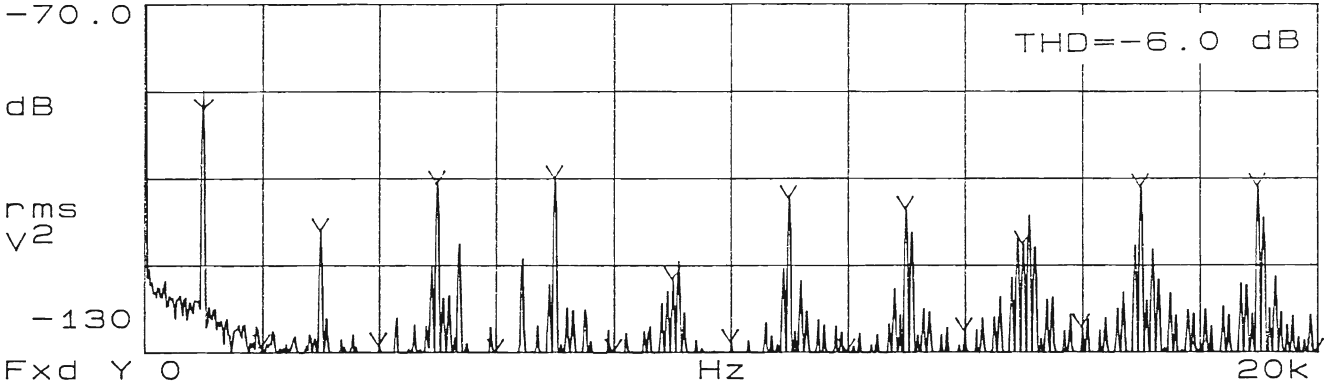
MEASUREMENT RESULTS

MULTIBIT
VS
BITSTREAM

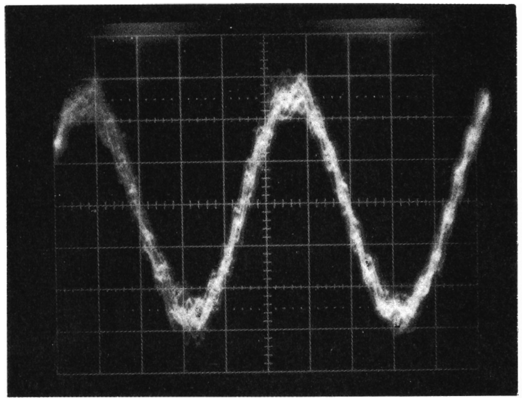
WAVEFORM AND HARMONIC DISTORTION

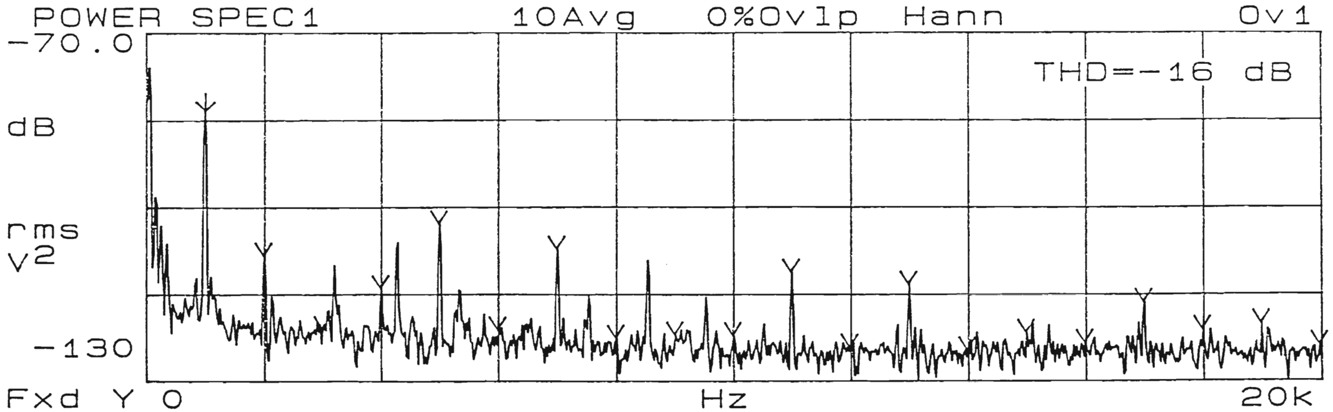
-80dB, 1kHz INPUT SIGNAL





A) CONVENTIONAL MULTIBIT CONVERSION

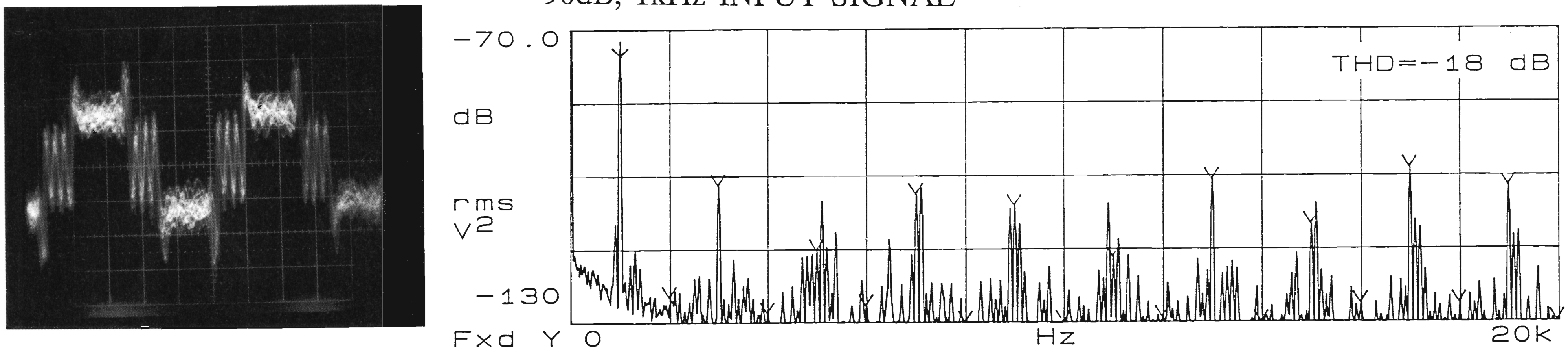




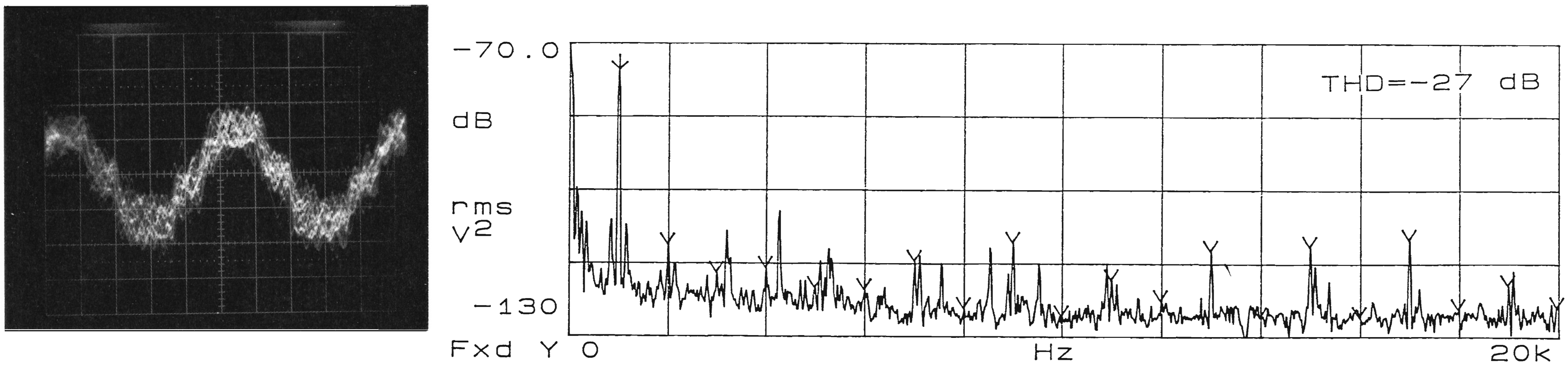
B) BITSTREAM CONVERSION

WAVEFORM AND HARMONIC DISTORTION

-90dB, 1kHz INPUT SIGNAL



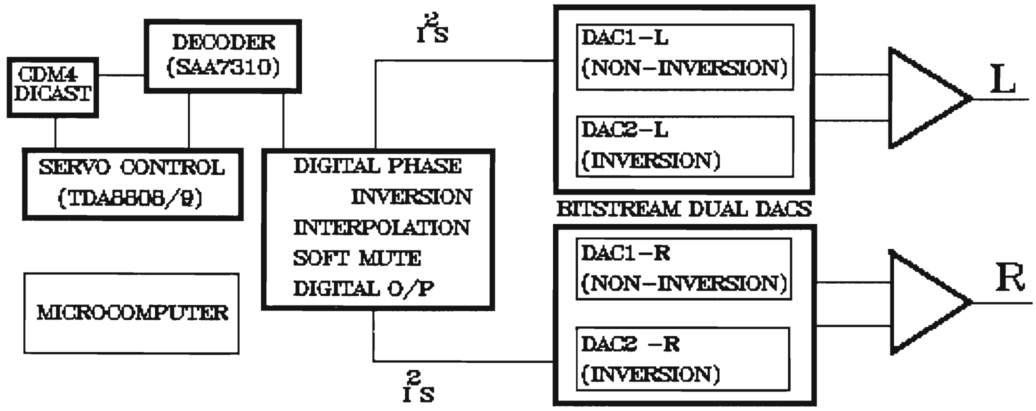
A) CONVENTIONAL MULTIBIT CONVERSION



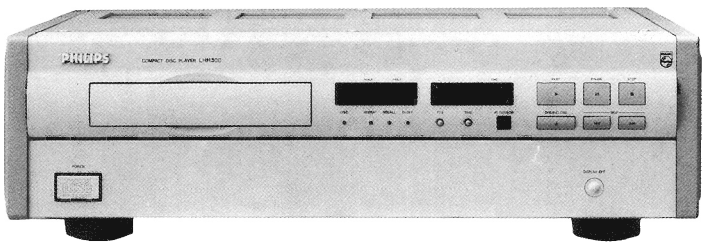
B) BITSTREAM CONVERSION

BITSTREAM DIFFERENTIAL MODE APPLICATION

Block Diagram



EXAMPLE : LHH500 PHILIPS CD PLAYER



LHH500 has won 6 awards in Japan for its sound quality performance.

Radio Gijyutsu	"'89 Components of the Year"
Stereo Sound F	"'89 Compo Grand Prix Prize" (CD player category)
Monthly Stereo	"'89 Best Buy Compo" (CD player category)
Audio & AV Special	"'89 Audio Masterpiece Prize" (CD player category)
Swing Journal	"'89 Jazz Component Award" (Forcign produced category)
Musen & Jikken	The 8th "Technology of the Year '89" (CD player category)

SUMMARY

OF

COMPONENTS

A/D, D/A CONVERTERS FROM PHILIPS

MULTIBIT CONVERTERS

Device	Function	S/N+THD (OdB 1KHz)	Supply Voltage	Package	Status
TDA 1541A R1 TDA 1541A std TDA 1541A S1	Dual D/A Dual D/A Dual D/A	>90 dB >90 dB >90 dB	: ±5v, −15v : ±5v, −15v : ±5v, −15v	DIL 28	NOW
TDA 1543 TDA 1543 A	Dual D/A Dual D/A	>70 dB >70 dB	: +5v : +5v	DIL 8 DIL 8	NOW NOW
TDA 1542	(Dual LPF+ Head Phone AMPLIF1ER)	>100 dB	: −5v, 12v −12v	DIL 28	NOW

BITSTREAM CONVERTERS

Device	Function	S/N+THD (OdB 1KHz)	Supply Voltage	Package	Status
SAA 7320	Dig, Fil+ Dual D/A+ Dual LPF 256 FS	>90 dB	: +5v	QFP 44	NOW
SAA 7321	Dual LPF (IMPROVED)	>90 dB	: +5V	QFP 44	NOW
SAA 7340	CD Decoder+ Dig, Fil.+ Dual D/A+ Dual LPF 192 FS	>80 dB	: +5v	QFP 80	QS
PCF 5022 + PCF 5023	Dig, Fil.+ Quad D/A+ 256 F9 Dual A/D 64 FS	>90 dB >84 dB	: +5v	PLCC 44	DEV.

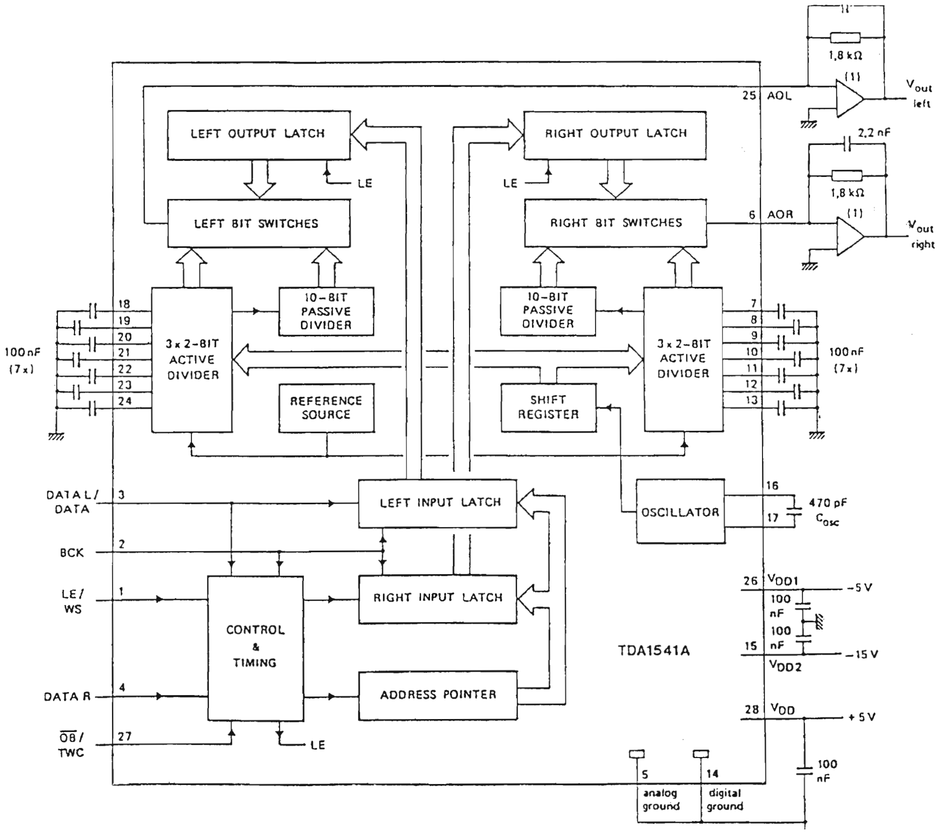
TDA 1541 A   Dual 16bit DAC

3 Versions

• relaxed	TDA 1541A R1	bit 1−16,	DLE < 2 LSB.
• standard	TDA 1541A	bit 1−16,	DLE < 1 LSB.
• Gold Crown	TDA 1541A S1	bit 1−7,	DLE < 0.5 LSB.
	bit 8−15,		DLE < 1 LSB.
		bit 16,	DLE < 0.75 LSB.

Differential linearity error (DLE)

Block Diagram



Features

• • Selectable two-channel input format : offset binary or two's complement.

• Internal timing and control circuit..

• TTL compatible digital inputs.

• High maximum input bit-rate and fast setting time. (UP TO 8F3)

• No requirement for external deglitcher circuit.

Application

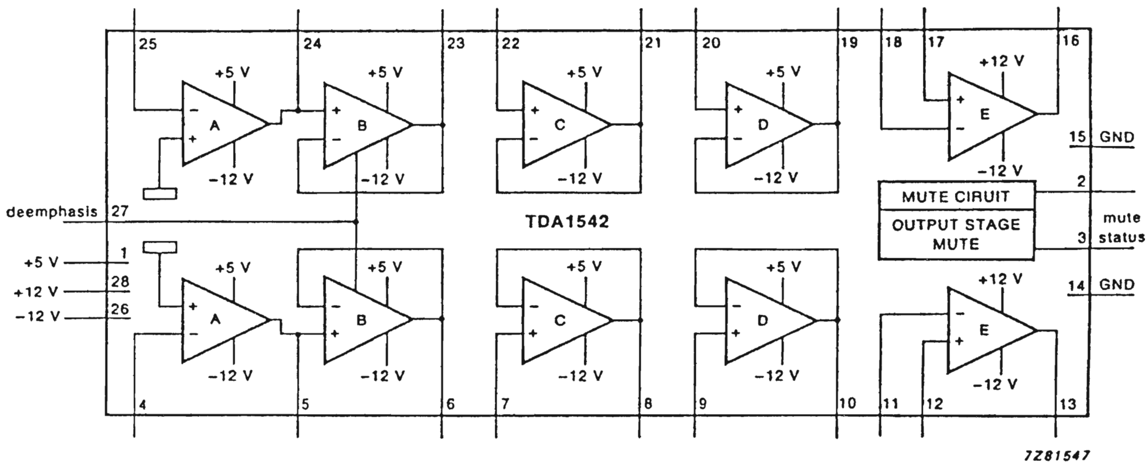
CD Player,   DAT, Satellite receiver

TDA 1542 High performance analog filter IC.

Features

- Flexibility of filter (3rd order LPF or more).
- Headphone driver with high out put and variable gain.
- Low distortion.
- Channel separation.
- High slew rate input amplifier.
- Mute deemphasis control.
- Line out adjustable output.
- Power ON／OFF mute.

Block diagram



Application

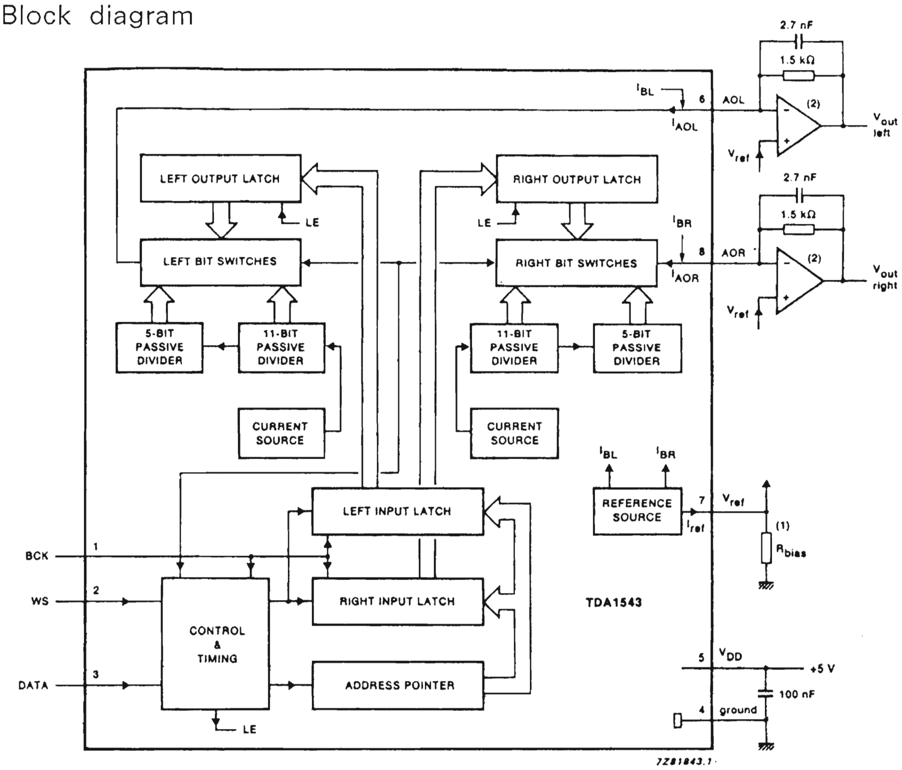
CD Player, DAT, Satellite receiver

TDA 1543 Dual 16 bit DAC

Features

- Low distortion
- 16 bit dynamic range
- 4×oversampling
- Single 5V power supply
- No external components required
- No requirement for external deglitcher circuitry due to fast settling output current
- Adjustable bias current
- Internal timing and control circuits
- Time multiplexed, 2's complement
- I^2S input format :
- S format : TDA 1543 A (2 versions)

Block diagram



Application

Portable CD, DAT, mini compo

Characteristics

supply voltage, current	+5V、50mA
S/N+D	75dB typ
input bit rate (pin3)	6.4Mbits/sec
clock freq.(pin1)	6.4MHz MAX
operating ambient temp. range	−30℃∼+85℃
bias current	−0.5∼1.8mA

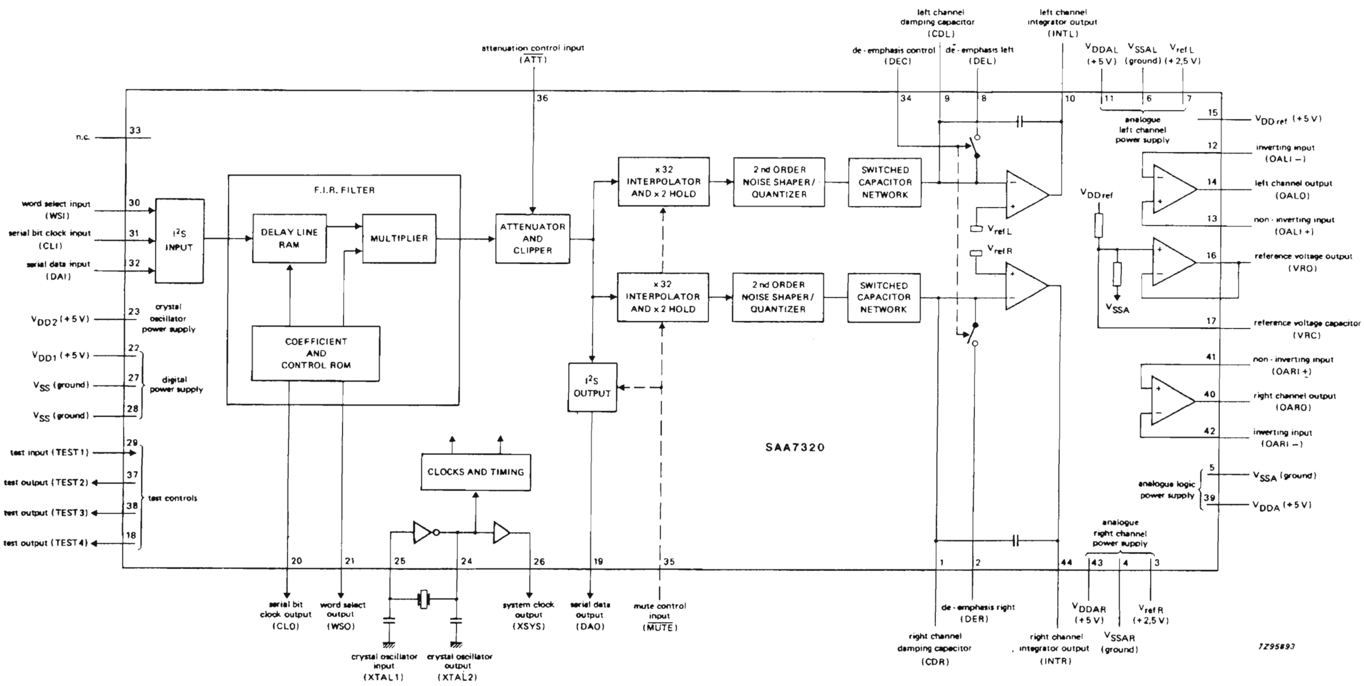
BITSTREAM DUAL D／A CONVERSION

SAA 7321 (STEREO CMOS DAC)

Features

- I^2S flexible data input
- Phase linear F.I.R. digtal filter with 1st order noise shaper
- 256 times over sampling by linear interpolation and sample hold
- 2nd order wide bus noise shaper
- 16 bit super linear resolution
- Switch capacitor 1 bit converter
- 3rd order low-pass filter to reduce out-of-band noise
- −12dB attenuation, de-emphasis and mute control
- Low power consumption (typ. 300mW)
- Single supply operation (+5V)
- Operating ambient temperature range of −40℃～+85℃

Block diagram SAA7320,SAA7321



Characteristics

- Dynamic range — 96 dB typ
- Distortion — under 90 dB
- Pass-band ripple — with in 0.035 dB
- Stop-band suppressio — over 60 dB
- Power supply — +5V ±10%
- P • D Dissipation — 300mW
- Package — 44pin QFP

BITSTREAM QUAD D/A, DUAL A/D CONVERTER

PCF 5022 (CMOS ANALOG・INTERFACE CIRCUIT・DIGITAL SECTION)

Features

- CMOS technology
- Single 5V supply
- I^2S data output/input
- 64×downsampling analog-to-digital conversion using 2 finite impulse response (FIR) filter stages giving a signal-to-noise ratio of > 84 dB
- 256×oversampling digital-to-analog conversion
- Digital-to-analog conversion including 2nd order noise shaping to give a signal-to-noise ratio of > 90 dB
- Mute control
- Operating ambient temperature range of −40℃～+85℃

Application

Digital Audio

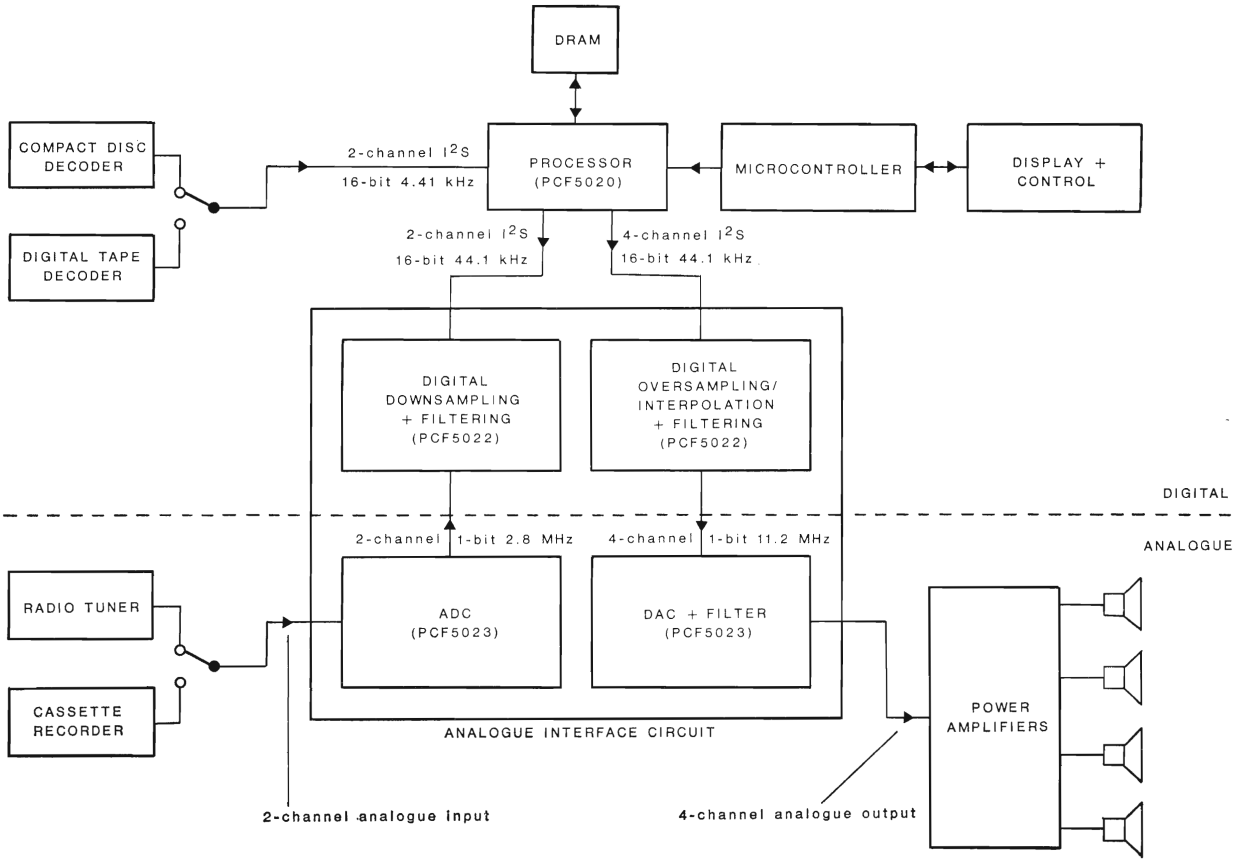
PCF 5023 (CMOS ANALOG・INTERFACE CIRCUIT・ANALOGUE SECTION)

Features (PCF−5023)

- CMOS technology
- Single 5V supply
- Reference voltage internally generated
- Low peripheral component count
- Stereo AtoD, quad DtoA
- 1 bit switched capacitor ADC with noise shaping to give 14 bit resolution
- 16-bit resolution from a 1-bit DAC, using switched capacitor integrator
- No external filtering required
- Operating ambient temperature range of −40℃～+85℃

Application

Digital Audio



Block diagram of Diagital Audio amplifier system.

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