TENTATIVE DEVICE SPECIFICATION

D1·6

28-04-83

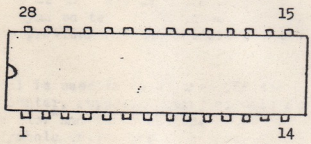
TYPE: Commercial No. SAA ~~7010~~ 7011
Development No. M4290A

FUNCTION; DEMODulator for Compact Disc Digital Audio System
(see Appendix I for System Description)

PROCESS: N-MOS

SUPPLY VOLTAGE: 5V ± 10% 12V ± 10% -2.5V ±0.5V

PACKAGE: 28 pin Plastic SOT 117A
Cerdil SOT 87B



Pin Configuration:

Pin	Signal	Type	Pin	Signal	Type
1	VBB	supply	15	VDD2	Supply
2	SDATA	output	16	OA1	input
3	SBCL	output	17	OA2	input
4	SWCL	output	18	OA3	output
5	P	output	19	VSS ANALOGUE	supply
6	HFD	input	20	VCO1	input
7	HFI	input	21	VCO2	output
8	$\overline{\text{HFI}}$	input	22	$\overline{\text{CEFM}}$	output
9	$\overline{\text{FB}}$	output	23	FD	output
10	FB	output	24	$\overline{\text{FSDE}}$	output
11	DEFM	output	25	$\overline{\text{SSDE}}$	output
12	PD2	output	26	$\overline{\text{CLDE}}$	output
13	PD1	output	27	DADE	output
14	VSS DIGITAL	supply	28	VDD1	supply

		FUNCTION: Compact Disc Demodulator	COMM: SAA 7010 EXP: M4290 A	DATE	3.2.82 23.2.82 16.11.82 08.04.83
		ISSUED BY: D. Braithwaite	1 Sh Sc 19	13.7.82	14.4.83

PHILIPS ELECTRONICS LIMITED SOUTHAMPTON

GENERAL DESCRIPTION: (see Block Diagram - Figure 1)

The M4290 Demodulator I.C. forms the front-end of the Compact Disc Digital Audio decoding system, supplying demodulated data and timing signals to the Error Corrector M4280 and the subcoding microprocessor.

The detected signal from the disc is amplified and filtered externally and then converted to a digital signal via the level detector. This is an adaptive data slicer which relies on the nature of the modulation system to determine the optimum slicing level.

A frequency detector and a phase detector provide the coarse and fine control signals for the phase locked loop (PLL) system. The gain is supplied by an internal operational amplifier which drives a voltage controlled oscillator (VCO) running at twice the input data rate which is nominally 4.3218MHz. The oscillator output is divided by 2 within the main clock generator which then clocks the input shift register and the timing chain. This clock signal completes the PLL loop when it is compared with the incoming data in the phase detector.

After the phase detector the data is clocked into the 23 bit input shift register to enable the frame sync pattern to be detected. Also, a minimum and maximum data length detector provides frequency limit signals (Tmin and Tmax) for the frequency detector.

The frame sync. signal is used to reset the ÷588 slave counter which, together with a ÷17 symbol rate counter, supplies timing signals for clocking the Eight to Fourteen Modulation (EFM) decoder* and the subcoding outputs. The data is read from the input shift register in symbols of 14 bits which are latched and then decoded into 8 bit data words. The subcoding part consists of only one word per frame (see Figure 2), therefore the output (SDATA) is a burst of 8 bits of data accompanied by a 2.1609MHz burst clock signal (SBCL) - see Figure 4. One bit of this subcoding output data is replaced by a subcoding frame sync bit (SF) which is decoded from either of two special EFM codes. The displaced bit is known as the Pause or P bit and is latched to its own output via a debounce circuit to remove erroneous changes.

The ÷588 slave counter also provides a sync. coincidence pulse which occurs when two detected sync pulses are precisely one frame length apart (588 clock cycles). This is used by the lock indication counter as an 'in-lock' signal to reset the counter and disable the frequency detector output (FD). If the system goes out of lock for any reason and the sync. pulses cease then the lock indication counter will count frame periods and after 63 frames will enable the frequency detector output.

The sync. coincidence pulse is also used via a delay line to reset the protected ÷588 master counter. The counter is prevented from accidental reset by erroneous sync. patterns by accepting only coincident sync. pulses or sync. pulses which occur during a predetermined 'window' at the beginning of each frame. This window is wide enough to allow for PLL bit slips, but narrow enough to avoid false sync. signals generated by corrupt data.

The ÷588 master counter, together with a second ÷17 symbol rate counter, is used to time the data and clock signals to ERCO (see Figure 3). In this way, even if the data has been corrupted, the timing signals are correct and only re-synchronised after a complete frame has been sent to the Error Corrector.

The data to ERCO (DADE) consists of 32 8-bit symbols per frame with half bit gaps between each symbol and a much longer gap during the frame sync. period. It is this longer gap that will change in length when corrupt data upsets the timing system

* see Appendix II

		FUNCTION: Compact Disc Demodulator	COMM: SAA 7010	DATE	08.03.82
			EXP: M4290 A	16.11.81	13.7.82
				3.2.82	14.4.83
		ISSUED BY: D. Braithwaite	2 SH SH 19		

PIN DESCRIPTION

Pin No.	Name	Description
1	VEB	-2.5V. Back Bias Supply.
2	SDATA	Push-pull output for subcoding data. An 8 bit burst of data (including a 1 bit subcoding frame sync) is output serially once per frame coincident with SBCL (see Figure 4)
3	SBCL	Push-pull output for subcoding bit clock. An 8 bit burst clock at nominally 2.1609MHz which is used to sychronise the subcoding data (see Figure 4).
4	SWCL	Push-pull output for subcoding word clock. A square wave signal at data frame rate (7.35KHz) used to synchronise the subcoding words and the pause (P) bit. (see Figure 4)
5	P	Push-pull output for the subcoding Pause bit. This signal is derived from the encoded subcoding word and is used to indicate a music pause. A debounce circuit is incorporated to eliminate erroneous data. (see Figure 4)
6	HFD	Input from external High Frequency Detector. When this signal is high the frequency detector output (FD) and phase detector are enabled.
7	HFI	Non-inverting input to the Level Detector. A differential signal of between 0.5V and 2.5V peak-peak is required between pins 7 and 8 drive the Level Detector correctly.
8	$\overline{\text{HFI}}$	Inverting input to the Level Detector.
9	$\overline{\text{FB}}$	Inverted feedback output from the Level Detector. These outputs ($\overline{\text{FB}}$ and FB) have a nominal impedance of 10KΩ and will default to ½ VDD1 when a drop-out is sensed.
10	FB	Non-inverted feedback output from the Level Detector (see $\overline{\text{FB}}$).
11	DEFM	Push-pull output for EFM data after it has passed through the level detector.

Pin No.	Name	Description
12	PD2	Phase detector reference signal. (see PD1)
13	PD1	Phase detector output signal. These outputs (PD1 and PD2) have a nominal impedance of 10 KΩ and the differential dc content of the signals is a measure of the phase difference between the data and the internal 4.3218MHz clock.
14	VSSD	Digital Ground. Main ground terminal
15	VDD2	+12V supply.
16	OA1	Non-inverting input to the Operational Amplifier.
17	OA2	Inverting input to the Operational Amplifier.
18	OA3	Source follower output of Operational Amplifier.
19	VSSA	Analogue Ground. Ground terminal for Operational Amplifier only. Connected internally to VSSD via a nominal 25Ω resistor.
20	VCO1	Input to Voltage Controlled Oscillator amplifier. The amplifier is a simple inverter designed for up to 10MHz operation. The frequency control is achieved via an external 'Varicap' tuned circuit.
21	VCO2	Output from Voltage Controlled Oscillator amplifier. The load for the inverting transistor may be turned off for test purposes by reducing VDD2 to 0V.
22	$\overline{\text{CEFM}}$	A push-pull output from the internal 4.3218MHz clock generator.
23	FD	Three state push-pull output from the Frequency Detector. This output has a nominal 1KΩ impedance when active but assumes a high impedance state once the system is in lock.
24	FSDE	Push-pull output for Frame Sync signal to ERCO. A positive going pulse occurring at the end of each data frame (nominal frequency 7.35KHz). (See Figure 3)
25	$\overline{\text{SSDE}}$	Push-pull output for Symbol Sync. signal to ERCO. A negative going pulse occuring during the last bit of each data symbol (nominal frequency 254KHz) (See Figure 3)

Pin No.	Name	Description
26	CLDE	Push-pull output for Data bit clock to ERCO. An 8 bit burst clock at nominally 2.1605MHz which is used to synchronise the data to ERCO (see Figure 3).
27	DADE	Push-pull output for Data to ERCO. Serial data consisting of 32 x 8 bit symbols per frame which is synchronised to $\overline{\text{CLDE}}$. (See Figure 3)
28	VDD1	+5V Supply.

		FUNCTION:	COMM:	DATE	08.03.82
		Compact Disc Demodulator	EXP: M4290A		13.7.82
		ISSUED BY:	5 SH SH 19	16.11.81	14.4.83

Electrical Characteristics

Absolute Ratings (VSSA = VSSD = 0V)

	Symbol	Value min	Value typ	Value max	Unit
Operating ambient temperature	Tamb	-20		+70	°C
Storage temperature	Tstg	-55		+125	°C
Back Bias Supply Voltage	VBB	-4.0		+0.3	V
Supply Voltage 1	V_{DD1}	-0.3		+7.5	V
Supply Voltage 2	V_{DD2}	-0.3		+15	V
Input Voltage	V_I max	-0.3		+7.5	V
Output Voltage (except FD, OA3)	V_O max	-0.3		+7.5	V
Output Voltage (FD, OA3 only)	$V_{O(FD,OA3)}$ max	-0.3		+15	V
Output current (each output)	Io max			10	mA
Electrostatic handling (equivalent to discharging a 250pF capacitor through a 1KΩ series resistor)	V_{ES}	-1000		+1000	V

Electrical Characteristics			Value			
Operating	Note	Symbol	Min.	Typ.	Max.	Unit
The following applies for Tamb = -20°C to +70°C and $V_{SSA} = V_{SSD} =$ 0 volt						
Back Bias Supply Voltage		VEB	-3.0	-2.5	-2.0	V
Supply Voltage 1		VDD1	4.5	5.0	5.5	V
Supply Voltage 2		VDD2	10.8	12.0	13.2	V
Supply Current 1		IDD1	~~30~~	tbn	150	mA
Supply Current 2		IDD2	~~4~~	tbn	21	mA
Back Bias Supply Current		IEB			-500	µA
Total Power Dissipation		PD		500		mW
The following applies for: Tamb = -20°C to +70°C VDD1 = 4.5V to 5.5V VDD2 = 10.8V to 13.2V VSSA = VSSD = ØV VEB = -2.0V to -3.0V unless otherwise stated						
INPUT: HFD/						
Input voltage low		V_{IL}	-0.3		0.8	V
Input voltage high		V_{IH}	2.4		6.5	V
Input current	(1)	I_{IN}	-1		+1	µA
Input capacitance		C_{IN}			7	pF
OUTPUTS: DADE/DEFM, $\overline{CLDE}$, FSDE, $\overline{SSDE}$, SBCL, SDATA, P, SWCL, CEFM	(2)					
Output Voltage low at I_{OL} = -1.6mA		V_{OL}	0		0.4	V
Output Voltage high at I_{OH} = 0.2mA		V_{OH}	3.0		VDD1 +0.5	V
Load Capacitance		C_L			150	pF
OUTPUT: FD						
Output Voltage low at I_{OL} = -100µA		V_{OL}	0		0.5	V
Output Voltage high at I_{OH} = 100µA		V_{OH}	8		VDD2 +0.5	V
Output leakage current for V_O = 0 - 6V	(3)	I_{LE}	-1		+1	µA
Output Impedance		Z_O		1		KΩ

	FUNCTION: Compact Disc Demodulator	COMM: SAA 7010	DATE	3.2.82	
		EXP: M4290 A		25.2.82	
			16.11.81	08.03.82	
	ISSUED BY: D. Braithwaite	7 SH SH 19	13.7.82	14.4.83	

Electrical Characteristics Operating	Note	Symbol	Value Min.	 Typ.	 Max.	Unit
OUTPUTS: PD1, PD2 (see figure 8)						
Output Impedance		Z_O		15		KΩ
Output Impedance matching		$\frac{Z_{O1}-Z_{O2}}{Z_{O1}+Z_{O2}}$			±10	%
Phase Detector control range		θ_e	-2.1		+2.1	rad
Phase Detector gain factor	(15)	Kd		0.16		V/ra
Common mode output voltage	(15)	Vdcm		4		V
ANALOGUE CIRCUIT CHARACTERISTICS Input Level Detector						
INPUTS: HFI, $\overline{HFI}$						
Input voltage range (AC)		V_{IAC}	1.0		2.5	Vp-p
Input Offset voltage		V_{IOF}	-25		+25	mV
Input current	(1)	I_{IN}	-1		+1	µA
Input offset current	(4)	I_{IDF}	-0.2		+0.2	µA
Input capacitance		C_{IN}			7	pF
Common mode input voltage ~~range~~		V_{ICM}	~~tbf~~	$\frac{1}{2}V_{bb1}$	~~tbf~~	V
OUTPUTS: FB, $\overline{FB}$						
Output impedance		Z_O		10		KΩ
Small signal gain at 500KHz (C_L=5pf)		Av	60			V/V
Output voltage high	(16)	Voh	4			V
Output voltage low	(17)	Vol			1	V
Feedback voltage with respectto ½ VDD1 (VDD1 = 5v, VDD2 = 12v, Tamb = 25°C)	(19)	Vfb	-70		-170	mV
PLL FILTER OP AMP	(5)					
INPUTS: OA1, OA2						
Common-mode voltage range		V_{ICM}	1.5		6	V
Input offset voltage		V_{IOF}	-30		+30	mV
Input current	(1)	I_{IN}	-1		+1	µA
Input offset current	(4)	I_{IOF}	-0.1		+0.1	µA

Characteristics	Notes	Symbol	Limits			Units
			min.	typ.	max.	
Input capacitance		C_{IN}			7	pF
CMR ratio			40			dB
Open loop gain (DC)			40			dB
Gain Bandwidth product (20dB/decade roll off)			1	5		MHz
OUTPUT: OA3						
Output voltage low at I_{OL} = -1mA		V_{OL}	0		1	V
Output voltage high at I_{OH} = 1mA		V_{OH}	8		VDD2 +0.5	V
VCO AMPLIFIER VCO1, VCO2						
Mutual conductance at 100KHz	See Fig 9	gm	1.5			mA/V
Bandwidth (-3dB cut off frequency)	See Fig 9	Bgm	20			MHz
Input capacitance		C_{IN}			7	pF
Output capacitance		C_{OUT}			7	pF
Feedback capacitance		C_{FB}			5	pF
Input leakage	(1)	I_{IN}	-1		+1	µA
Output current (at 10MHz)		Iout	-1		+1	mA
Small signal voltage gain at 100KHz	See Fig 9	A_V	4			V/V
TIMING						
Operating frequency (except VCO)		Fcefm	0.1		5	MHz
Operating frequency (VCO only)		Fvco	0.2		10	MHz
OUTPUTS: $\overline{CLDE}$, DADE , $\overline{SSDE}$, FSDE, $\overline{CEFM}$ (see Figure 5)	(6,12)					
Output rise time		t_{OR}			50	ns
Output fall time		t_{OF}			40	ns
$\overline{CLDE}$ period		t_{OCP}	400			ns
$\overline{CLDE}$ high time		t_{OCH}	150			ns
$\overline{CLDE}$ low time		t_{OCL}	150			ns
DADE/$\overline{SSDE}$/FSDE to $\overline{CLDE}$ set up		t_{ODS}	100			ns
$\overline{CLDE}$ to DADE/$\overline{SSDE}$/FSDE hold		t_{ODH}	100			ns
$\overline{SSDE}$ low time	(7)	t_{SSL}		3		$\overline{CEFM}$ period
$\overline{CLDE}$ low time during FSDE	(8)	t_{OCG}	16	46 ~~47~~		$\overline{CEFM}$ period
$\overline{CLDE}$ to $\overline{CEFM}$ set up		t_{ODSE}		100		nsec
$\overline{CEFM}$ to $\overline{CLDE}$ hold		t_{ODHE}		100		nsec

FUNCTION:	COMM: SAA 7010	DATE	23.2.82	
Compact Disc Demodulator	EXP: M4290A	16.11.81	08.03.82	13.7.82
ISSUED BY: D. Braithwaite	9 SH SH 19	3.2.82		
MULLARD LIMITED SOUTHAMPTON		14.4.83		

Electrical Characteristics Operating - timing	Notes	Symbol	Value min	 typ	 max	Unit
OUTPUTS: SBCL, SDATA, P, SWCL (see Figure 6)	(12,13, 14)					
Output rise time (SBCL, SDATA)	(6)	t_{OR}			50	ns
Output fall time (SBCL, SDATA)	(6)	t_{OF}			40	ns
Output rise time (P, SWCL)	(9)	t_{OSR}			200	ns
Output fall time (P, SWCL)	(9)	t_{OSF}			200	ns
SBCL high time		t_{OCH}	150			ns
SBCL low time		t_{OCL}	150			ns
SDATA to SBCL set up		t_{ODS}	100			ns
P to SWCL set up		t_{ODSP}	1			µs
SBCL to SDATA hold		t_{ODH}	100			ns
SBCL to SWCL hold		t_{SWH}	0		500	ns
SWCL Duty cycle (t_{high}/t_{period})			40	50	60	%
OUTPUT: FD	(12)					
Output rise time	(6)	t_{FDR}			1	µs
Output fall time	(6)	t_{FDF}			1	µs
OUTPUTS: DEFM, $\overline{\text{CEFM}}$ (see Figure 7)	(6,12)					
Output rise time		t_{OR}			50	ns
Output fall time		t_{OF}			40	ns
DEFM to $\overline{\text{CEFM}}$ set up	(18)	t_{ODS}	50			ns
$\overline{\text{CEFM}}$ to DEFM hold	(18)	t_{CDH}	70			ns
$\overline{\text{CEFM}}$ high time		t_{OCH}	50			ns
$\overline{\text{CEFM}}$ low time		t_{OCL}	50			ns

NOTES

1. Vin -0.3 to 6.5V, 25°C, measured with VDD1 = 6.5V
2. short circuit protected to VDD1 and VSS. The maximum load capacitance that can be applied before short circuit protection becomes operative is 150pF.
3. output in high impedance state 25°C.
4. 25°C
5. all tests done within common mode voltage range
6. output loading 50pF
7. $\overline{\text{SSDE}}$ reamins low for only one negative edge of $\overline{\text{CLDE}}$
8. excessive bit-slip may cause gap to disappear
9. output loading 150pF
10. the SYNC bit is low when a subcoding sync word is detected.
11. $\overline{\text{CLDE}}$ remains low when FSDE is high
12. reference levels are 0.8V and 2.4V
13. output loading 50pF for SBCL and SDATA, and 150pF for SWCL and P
14. SWCL has a 50% duty cycle.
15. Average data run length = 5x CEFM periods
16. 100kΩ connected between output and VSS, VDD1 = 5V
17. 100KΩ connected between output and VDD1, VDD1 = 5V
18. Free running VCO frequency tunned to nominal & PLL in lock with a typical application circuit is shown in Figure 1.
19. Measured with Viac = 1v p-p undistorted EFM signal

		FUNCTION: Compact Disc Demodulator	COMM: SAA 7010	DATE	23.2.82
			EXP: M4290A	3.2.82	08.03.82
		ISSUED BY: D. Braithwaite	11 SH SH 19	13.7.82	14.4.83
		PHILIPS MULLARD LIMITED SOUTHAMPTON			

FIG 1

FUNCTION: COMPACT DISC DEMODULATOR BLOCK DIAGRAM	COMM: SAA 7010	DATE	16/11/81
	EXP: M4290A	14-4-83	08.03.82
ISSUED BY: D. Braithwaite	12 SH 2 SH 19		13.7.82

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FIGURE 2 - HF Input Waveform

	FUNCTION: Compact Disc Demodulator	COMM: SAA 7010	DATE	08.03.82
		EXP: M4290 A	3.2.82	13.7.82
	ISSUED BY: D. Braithwaite	13 SH SH 19	23.2.82	14.4.83
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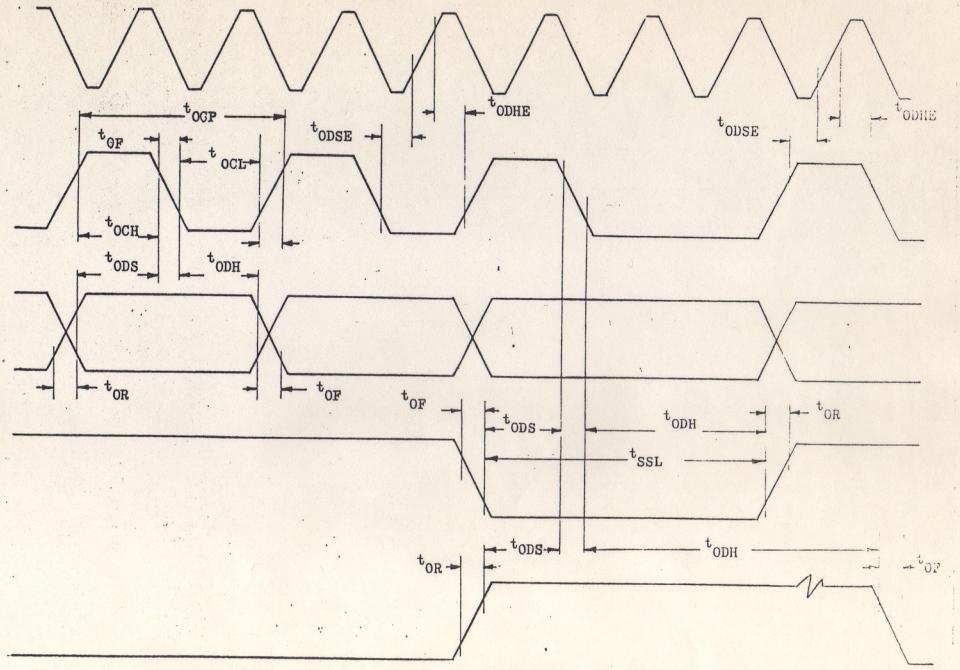
FIGURE 3 - Output Waveforms (To ERCO)

FIGURE 4 - Output Waveforms (Subcoding)

FUNCTION: Compact Disc Demodulator	COMM: SAA 7010	DATE	08.03.82
	EXP: M4290A	3.2.82	13.7.82
ISSUED BY: D. Braithwaite	14 SH SE 19	23.2.82	14.4.83

FUNCTION: Compact Disc Demodulator	COMM: SAA7010
	EXP: M4290 A

	DATE
	14.4.83
	13.1.82
	08.03.82



See notes (6), (12)

Figure 5. Output Waveform Timing (to ERCO)

FIGURE 6 – Output Waveform Timing (Sub Coding)

	FUNCTION:	COMM: SAA 7010		DATE	08.03.82
	Compact Disc Demodulator	EXP: M4290 A		3.2.82	13.7.82
				23.2.82	14.4.83
	ISSUED BY: D. Braithwaite	16 SH	SH 19		

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FIGURE 7 - Output Waveform Timing (EFM outputs)

see notes 6, 12

		FUNCTION:	COMM: SAA 7010	DATE	08.03.82
		Compact Disc Demodulator	EXP: M4290 A	23.2.82	13.7.82
		ISSUED BY: D. Braithwaite	17 SH SH 19	14.4.83	
		MULLARD LIMITED SOUTHAMPTON			

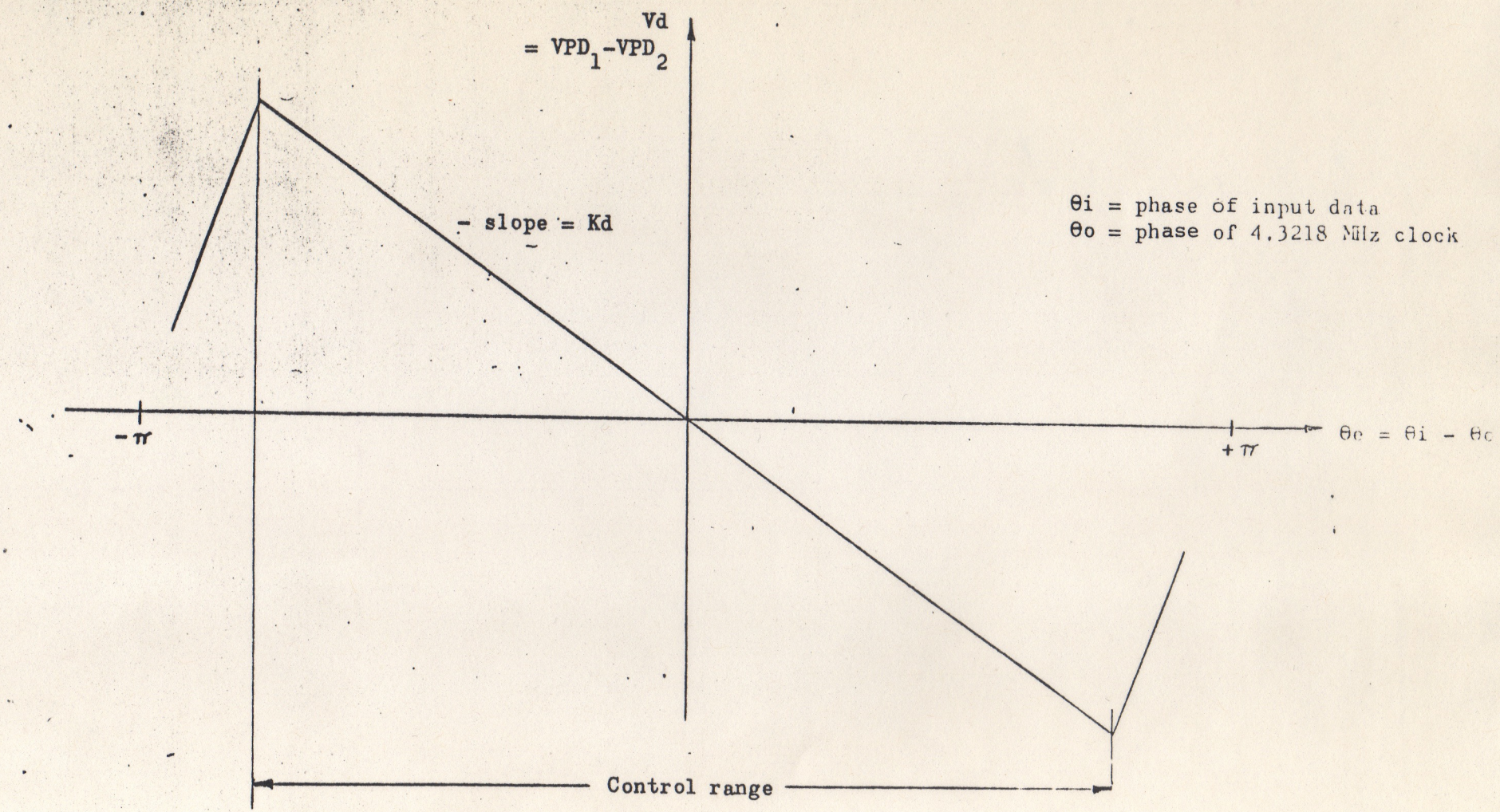
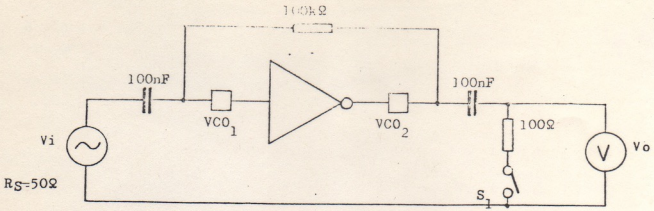


Figure 8 Typical Phase Detector Characteristic

ISSUED BY: D. Braithwaite	Disc Demodulator	FUNCTION: Compact	
I8 SH SH I9	EXP: M4290 A	COMM: SAA7010	
13.7.82	8.03.82		DATE
	14.4.83		

MULLARD LIMITED SOUTHAMPTON



S_1 closed to measure gm

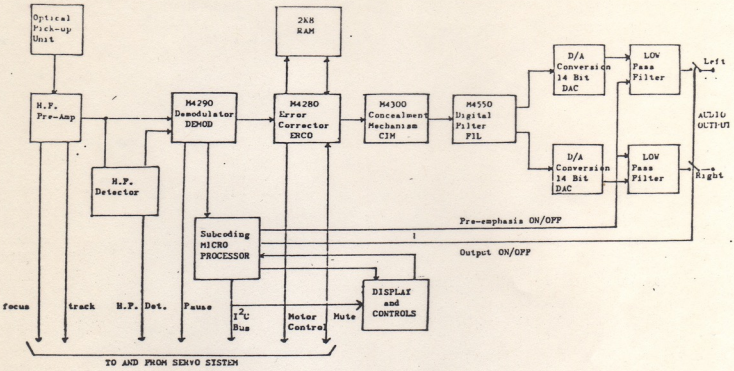
$$gm = \frac{Io}{Vi} = \frac{10xVo}{Vi} \quad mA/V$$

Figure 9. Measurement circuit for VCO voltage gain and gm

		FUNCTION: Compact Disc Demodulator	COMM: SAA7010	DATE 8.03.82	14 4 83
			EXP: M4290 A	13.7.82	
		ISSUED BY: D. Braithwaite	19 SH SH 19		
		ULLARD LIMITED SOUTHAMPTON			

APPENDIX I

Simplified Block Diagram for the Compact Disc Digital Audio System



SYSTEM DESCRIPTION

The information contained in the pit structures on the disc is converted to a coded input signal via the Optical Pick-up Unit. This signal is amplified and filtered to remove the low frequency tracking information and to equalise the frequency response.

The M4290 DEMOD re-generates the data rate bit clock and timing signals from the H.F. input signal. This EFM modulated signal is decoded into a N.R.Z. form and the subcoding data extracted and fed to the external Subcoding Microprocessor. The decoded 8 bit data symbols are fed serially into the Error Corrector I.C. together with timing signals.

		FUNCTION: Compact Disc System	COM: EXP:	DATE 19.11.81
		ISSUED BY: D. Noble	1 SH SH 2	

The M4280 ERCO corrects up to two erroneous symbols per frame in the data received from DEMOD. The necessary de-interleaving to obtain the required data format is achieved by writing out the data in 8 bit parallel symbols to an external RAM and then reading it back in a defined sequence. After all possible corrections have been made the data is fed out of ERCO in a 16 bit serial format. A further function of ERCO is to re-synchronise the data to a steady 2.1168MHz clock rate derived from a 4.2336MHz crystal oscillator on the CIM I.C. This removes any jitter from the data while further operations eliminate wow and flutter plus any F.M. content in the data signal. If the ERCO is unable to correct error bits then the uncorrected data is passed to CIM together with an Unreliable Data warning signal.

The M4300 CIM accepts the 16 bit serial data and acts in such a way that, if the Unreliable Data signal is received, the effect of the errors is minimised. If the error results in a single unreliable sample then this is interpolated by replacing it by a new sample whose value is calculated from the values of the good sample immediately preceeding it and that succeeding it. If a string of unreliable samples is received then the output is muted by replacing unreliable samples with zero value samples and reducing the value of the thirty samples preceeding and succeeding them to smooth out the effects of the transition. The output of CIM is split into fourteen or sixteen bit stereo left or right data in Offset Binary or Twos Compliment format.

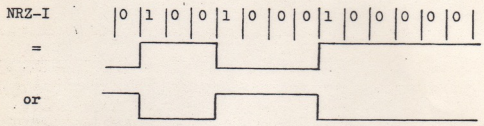
The M4550 FIL is a digital interpolating filter which improves the signal to noise ratio. It also enables a simpler analogue filter to be used after the Digital to Analogue Converter (DAC). The M4550 is a low pass digital transversal filter with 96 taps. The stereo output is organised in serial fourteen bit samples with the M.S.B. first. It is switchable between Offset Binary and Twos Compliment code. The output sample frequency is 176.4KHz which is four times the input sampling frequency.

APPENDIX 11

EFM Encoding System

The Eight to Fourteen Modulation (EFM) code used in the Compact Disc Digital Audio system is designed to restrict the bandwidth of the data on the disc and present a d.c. free signal signal to the demodulator. The actual number of bits per symbol is 17 which includes 3 merging bits which also help to remove the d.c. content.

Table 1 shows the conversion from 8 bit NRZ symbols to the equivalent 14 bit symbols. The 14 bit symbols are given in NRZ-I representation in which a 1 means a transistion at the beginning of that bit from high-low or low to high i.e.



C1 is the first bit of the 14 bit symbol read from the disc and D1 is the Most Significant Bit (MSB) of data which appears first at the DADE output from DEMOD.

The codes shown in Table 1 cover the normal 256 possibilities for an 8 bit data word. However, there are several other combinations of 14 bit codes which, although they obey the EFM rules for maximum and minimum run length, will produce unspecified output data symbols. Two of these extra codes are used in the subcoding data to define a subcoding frame sync.

These are:-

D1 ... D8	C1 ... C14
1 1 1 1 1 0 0 0	0 0 1 0 0 0 0 0 0 0 0 0 0 1
1 0 1 1 1 1 1 0	0 0 0 0 0 0 0 0 0 1 0 0 1 0
W V U T S R Q SYNC	

When a subcoding frame sync is detected the P bit of the data is ignored by the debounce circuitry. The remaining bits Q - W are not specified in the system but will always be as shown from this device.