

TENTATIVE DEVICE SPECIFICATION

D1-6

28-04-83

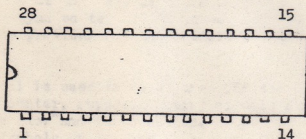
TYPE: Commercial No. SAA 7010
 Development No. M4290A

FUNCTION: DEMODulator for Compact Disc Digital Audio System
 (see Appendix I for System Description)

PROCESS: N-MOS

SUPPLY VOLTAGE: 5V ± 10% 12V ± 10% -2.5V ± 0.5V

PACKAGE: Plastic SOT 117A
 28 pin Cerdip SOT 87B



Pin Configuration:

| Pin | Signal | Type | Pin | Signal | Type |
|-----|-------------|--------|-----|--------------|--------|
| 1 | VBB | supply | 15 | VDD2 | Supply |
| 2 | SDATA | output | 16 | OA1 | input |
| 3 | SBCL | output | 17 | OA2 | input |
| 4 | SWCL | output | 18 | OA3 | output |
| 5 | P | output | 19 | VSS ANALOGUE | supply |
| 6 | HFD | input | 20 | VC01 | input |
| 7 | HFI | input | 21 | VC02 | output |
| 8 | HFI | input | 22 | CEFM | output |
| 9 | FB | output | 23 | FD | output |
| 10 | FB | output | 24 | FSDE | output |
| 11 | DEFM | output | 25 | SSDE | output |
| 12 | PD2 | output | 26 | CLDE | output |
| 13 | PD1 | output | 27 | DADE | output |
| 14 | VSS DIGITAL | supply | 28 | VDD1 | supply |

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|------------|--------------------------|----------------|----------|---------|
| FUNCTION: | Compact Disc Demodulator | COMM: SAA 7010 | DATE: | 3.2.82 |
| ISSUED BY: | D. Braithwaite | EXP: M4290A | 16.11.81 | 23.2.82 |
| | | 1 | SR | SR 19 |
| | | | 13.1.82 | 14.4.83 |

GENERAL DESCRIPTION: (see Block Diagram - Figure 1)

The M4290 Demodulator I.C. forms the front-end of the Compact Disc Digital Audio decoding system, supplying demodulated data and timing signals to the Error Corrector M4280 and the subcoding microprocessor.

The detected signal from the disc is amplified and filtered externally and then converted to a digital signal via the level detector. This is an adaptive data slicer which relies on the nature of the modulation system to determine the optimum slicing level.

A frequency detector and a phase detector provide the coarse and fine control signals for the phase locked loop (PLL) system. The gain is supplied by an internal operational amplifier which drives a voltage controlled oscillator (VCO) running at twice the input data rate which is nominally 4.3218MHz. The oscillator output is divided by 2 within the main clock generator which then clocks the input shift register and the timing chain. This clock signal completes the PLL loop when it is compared with the incoming data in the phase detector.

After the phase detector the data is clocked into the 23 bit input shift register to enable the frame sync pattern to be detected. Also, a minimum and maximum data length detector provides frequency limit signals (T_{min} and T_{max}) for the frequency detector.

The frame sync. signal is used to reset the ± 588 slave counter which, together with a ± 17 symbol rate counter, supplies timing signals for clocking the Eight to Fourteen Modulation (EFM) decoder and the subcoding outputs. The data is read from the input shift register in symbols of 14 bits which are latched and then decoded into 8 bit data words. The subcoding part consists of only one word per frame (see Figure 2), therefore the output (SDATA) is a burst of 8 bits of data accompanied by a 2.1609MHz burst clock signal (SBCL) - see Figure 4. One bit of this subcoding output data is replaced by a subcoding frame sync bit (SF) which is decoded from either of two special EFM codes. The displaced bit is known as the Pause or P bit and is latched to its own output via a debounce circuit to remove erroneous changes.

The ± 588 slave counter also provides a sync. coincidence pulse which occurs when two detected sync pulses are precisely one frame length apart (588 clock cycles). This is used by the lock indication counter as an 'in-lock' signal to reset the counter and disable the frequency detector output (FD). If the system goes out of lock for any reason and the sync. pulses cease then the lock indication counter will count frame periods and after 63 frames will enable the frequency detector output.

The sync. coincidence pulse is also used via a delay line to reset the protected ± 588 master counter. The counter is prevented from accidental reset by erroneous sync. patterns by accepting only coincident sync. pulses or sync. pulses which occur during a predetermined 'window' at the beginning of each frame. This window is wide enough to allow for PLL bit slips, but narrow enough to avoid false sync. signals generated by corrupt data.

The ± 588 master counter, together with a second ± 17 symbol rate counter, is used to time the data and clock signals to ERCO (see Figure 3). In this way, even if the data has been corrupted, the timing signals are correct and only re-synchronised after a complete frame has been sent to the Error Corrector.

The data to ERCO (DADE) consists of 32 8-bit symbols per frame with half bit gaps between each symbol and a much longer gap during the frame sync. period. It is this longer gap that will change in length when corrupt data upsets the timing system

* see Appendix II

| | | | |
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| FUNCTION: | COMP: SAA 7010 | DATE | 08.03.82 |
| Compact Disc Demodulator | EXP: M4290 A | 16.11.81 | 13.7.82 |
| ISSUED BY: D. Braithwaite | 2 SH SH 19 | 3.2.82 | 14.4.83 |

PIN DESCRIPTION

| <u>Pin No.</u> | <u>Name</u> | <u>Description</u> |
|----------------|-------------------------|--|
| 1 | VEB | -2.5V. Back Bias Supply! |
| 2 | SDATA | Push-pull output for subcoding data. An 8 bit burst of data (including a 1 bit subcoding frame sync) is output serially once per frame coincident with SBCL (see Figure 4) |
| 3 | SECL | Push-pull output for subcoding bit clock. An 8 bit burst clock at nominally 2.1609MHz which is used to synchronise the subcoding data (see Figure 4). |
| 4 | SWCL | Push-pull output for subcoding word clock. A square wave signal at data frame rate (7.35KHz) used to synchronise the subcoding words and the pause (P) bit. (see Figure 4) |
| 5 | P | Push-pull output for the subcoding Pause bit. This signal is derived from the encoded subcoding word and is used to indicate a music pause. A debounce circuit is incorporated to eliminate erroneous data. (see Figure 4) |
| 6 | HFD | Input from external High Frequency Detector. When this signal is high the frequency detector output (FD) and phase detector are enabled. |
| 7 | HFI | Non-inverting input to the Level Detector. A differential signal of between 0.5V and 2.5V peak-peak is required between pins 7 and 8 drive the Level Detector correctly. |
| 8 | $\overline{\text{HFI}}$ | Inverting input to the Level Detector. |
| 9 | $\overline{\text{FB}}$ | Inverted feedback output from the Level Detector. These outputs ($\overline{\text{FB}}$ and FB) have a nominal impedance of 10K Ω and will default to $\frac{1}{2}$ VDD1 when a drop-out is sensed. |
| 10 | FB | Non-inverted feedback output from the Level Detector (see $\overline{\text{FB}}$). |
| 11 | DEFM | Push-pull output for EFM data after it has passed through the level detector. |

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| ISSUED BY: D. Braithwaite | 3 SH SH 19 | 08.03.83 | |

| Pin No. | Name | Description |
|---------|------|---|
| 12 | PD2 | Phase detector reference signal. (see PD1) |
| 13 | PD1 | Phase detector output signal. These outputs (PD1 and PD2) have a nominal impedance of 10 K Ω and the differential dc content of the signals is a measure of the phase difference between the data and the internal 4.3218MHz clock. |
| 14 | VSSD | Digital Ground. Main ground terminal |
| 15 | VDD2 | +12V supply. |
| 16 | OA1 | Non-inverting input to the Operational Amplifier. |
| 17 | OA2 | Inverting input to the Operational Amplifier. |
| 18 | OA3 | Source follower output of Operational Amplifier. |
| 19 | VSSA | Analogue Ground. Ground terminal for Operational Amplifier only. Connected internally to VSSD via a nominal 25 Ω resistor. |
| 20 | VC01 | Input to Voltage Controlled Oscillator amplifier. The amplifier is a simple inverter designed for up to 10MHz operation. The frequency control is achieved via an external 'Varicap' tuned circuit. |
| 21 | VC02 | Output from Voltage Controlled Oscillator amplifier. The load for the inverting transistor may be turned off for test purposes by reducing VDD2 to 0V. |
| 22 | CEFM | A push-pull output from the internal 4.3218MHz clock generator. |
| 23 | FD | Three state push-pull output from the Frequency Detector. This output has a nominal 1K Ω impedance when active but assumes a high impedance state once the system is in lock. |
| 24 | FSDE | Push-pull output for Frame Sync signal to ERCO. A positive going pulse occurring at the end of each data frame (nominal frequency 7.35KHz). (See Figure 3) |
| 25 | SSDE | Push-pull output for Symbol Sync. signal to ERCO. A negative going pulse occurring during the last bit of each data symbol (nominal frequency 254KHz) (See Figure 3) |

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| Pin No. | Name | Description |
|---------|------|--|
| 26 | UPEE | Push-pull output for Data bit clock to ERCC. An 8 bit burst clock at nominally 2.160MHz which is used to synchronise the data to ERCC (see Figure 3). |
| 27 | DADE | Push-pull output for Data to ERCC. Serial data consisting of 32 x 8 bit symbols per frame which is synchronised to CLDE. (See Figure 3) |
| 28 | VDD1 | +5V Supply. |

| | | | | | |
|--|--|--|--------------------|-------------|----------|
| | | FUNCTION: Compact Disc Demodulator | CONH: | DATE | 08.03.82 |
| | | SUED BY: | EXP: M4290A | | 13.7.82 |
| | | | 5 SH SH 19 | 16.11.81 | 14.4.83 |

| Electrical Characteristics | Symbol | Value | | | Unit |
|---|----------------------------|-------|-----|-------|------|
| | | min | typ | max | |
| Absolute Ratings (VCEA = VCCD = μ V) | | | | | |
| Operating ambient temperature | T _{amb} | -20 | | +70 | °C |
| Storage temperature | T _{stg} | -55 | | +125 | °C |
| Back Bias Supply Voltage | V _{BB} | -4.0 | | +0.3 | V |
| Supply Voltage 1 | V _{DD1} | -0.3 | | +7.5 | V |
| Supply Voltage 2 | V _{DD2} | -0.3 | | +15 | V |
| Input Voltage | V _I max | -0.3 | | +7.5 | V |
| Output Voltage (except FD, OA3) | V _O max | -0.3 | | +7.5 | V |
| Output Voltage (FD, OA3 only) | V _{O(FD,OA3)} max | -0.3 | | +15 | V |
| Output current (each output) | I _o max | | | 10 | mA |
| Electrostatic handling (equivalent to discharging a 250pF capacitor through a 1k Ω series resistor) | V _{ES} | -1000 | | +1000 | V |

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FUNCTION:

Compact Disc Demodulator

COMM: SAA 7010

EXP: M4290 A

DATE

23.2.82

16.11.81 08.03.82

3.2.82 13.7.82

DESIGNED BY: D. Braithwaite

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14.11.82

Electrical Characteristics

Operating

The following applies for

$T_{amb} = -20^{\circ}C$ to $+70^{\circ}C$ and $V_{SSA} = V_{SSD} = 0$ volt

Back Bias Supply Voltage

Supply Voltage 1

Supply Voltage 2

Supply Current 1

Supply Current 2

Back Bias Supply Current

Total Power Dissipation

The following applies for:

$T_{amb} = -20^{\circ}C$ to $+70^{\circ}C$

VDD1 = 4.5V to 5.5V

VDD2 = 10.8V to 13.2V

VSSA = VSSD = \emptyset V

VBE = -2.0V to -3.0V

unless otherwise stated

INPUT: HFD/

Input voltage low

Input voltage high

Input current

Input capacitance

OUTPUTS: DADE/DEFM, CLDE, FSDE, SSDE, SBCL, SDATA, P, SWCL, CEFM

Output Voltage low at $I_{OL} = -1.6mA$

Output Voltage high at $I_{OH} = 0.2mA$

Load Capacitance

OUTPUT: FD

Output Voltage low at $I_{OL} = -100\mu A$

Output Voltage high at $I_{OH} = 100\mu A$

Output leakage current for $V_0 = 0 - 6V$

Output Impedance

| | | | | |
|------|---------------|------|------|---------|
| VBE | -3.0 | -2.5 | -2.0 | V |
| VDD1 | 4.5 | 5.0 | 5.5 | V |
| VDD2 | 10.8 | 12.0 | 13.2 | V |
| IDD1 | 30 | tbn | 150 | mA |
| IDD2 | 1 | tbn | 21 | mA |
| IBB | | | -500 | μA |
| PD | | 500 | | mW |

| | | | | |
|----------|------|--|-----|---|
| V_{IL} | -0.3 | | 0.8 | V |
| V_{IH} | 2.4 | | 6.5 | V |

| | | | | |
|----------|----|--|----|---------|
| I_{IN} | -1 | | +1 | μA |
| C_{IN} | | | 7 | pF |

| | | | | |
|----------|-----|--|--------------|---|
| V_{OL} | 0 | | 0.4 | V |
| V_{OH} | 3.0 | | VDD1 +0.5 | V |

| | | | | |
|-------|--|--|-----|----|
| C_L | | | 150 | pF |
|-------|--|--|-----|----|

| | | | | |
|----------|---|--|--------------|---|
| V_{OL} | 0 | | 0.5 | V |
| V_{OH} | 8 | | VDD2 +0.5 | V |

| | | | | |
|----------|----|--|----|---------|
| I_{LE} | -1 | | +1 | μA |
|----------|----|--|----|---------|

| | | | | |
|-------|--|---|--|------------|
| Z_0 | | 1 | | K Ω |
|-------|--|---|--|------------|

FUNCTION:
Compact Disc Demodulator

COMM: SAA 7010
EXP: M429 0 A

DATE
3.2.82
25.2.82
16.11.81
08.03.82

ISSUED BY: D. Braithwaite

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Electrical Characteristics

Outputs

OUTPUTS: PD1, PD2 (see figure 8)

Output Impedance

 Z_0

15

K Ω

Output Impedance matching

 $\frac{Z_{01} - Z_{02}}{Z_{01} + Z_{02}}$

+10

%

Phase Detector control range

 θ_e

-2.1

+2.1

rad

Phase Detector gain factor

(15)

Kd

0.15

V/rad

Common mode output voltage

(15)

Vdcm

4

V

ANALOGUE CIRCUIT CHARACTERISTICSInput Level DetectorINPUTS: HFI, $\overline{\text{HFI}}$

Input voltage range (AC)

V_{IAC}

1.0

2.5

V_{p-p}

Input Offset voltage

V_{IOF}

-25

+25

mV

Input current

(1)

I_{IN}

-1

+1

 μA

Input offset current

(4)

I_{IDF}

-0.2

+0.2

 μA

Input capacitance

C_{IN}

7

pF

Common mode input voltage ~~range~~V_{ICM}~~1.0~~ $\frac{1}{2} V_{DD1}$ ~~1.0~~

V

OUTPUTS: FB, $\overline{\text{FB}}$

Output impedance

 Z_0

10

K Ω Small signal gain at 500KHz ($C_L=5\text{pf}$)A_v

60

V/V

Output voltage high

(16)

V_{oh}

4

V

Output voltage low

(17)

V_{ol}

1

V

Feedback voltage with respect to $\frac{1}{2} V_{DD1}$
(V_{DD1} = 5v, V_{DD2} = 12v, T_{amb} = 25°C)

(19)

V_{fb}

-70

-170

mV

PLL FILTER OF AMP

(5)

INPUTS: OA1, OA2

Common-mode voltage range

V_{ICM}

1.5

6

V

Input offset voltage

V_{IOF}

-30

+30

mV

Input current

(1)

I_{IN}

-1

+1

 μA

Input offset current

(4)

I_{IOF}

-0.1

+0.1

 μA

FUNCTION:

Compact Disc Demodulator

COMM: SAA 7010

EXP: M4250 A

DATE

23.2.82

16.11.81

08.03.82

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13.1.82

ISSUED BY: D. Braithwaite

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| Electrical Characteristics | | Conditions | | | |
|--|---------------|------------|-----|-----------|-------------|
| Operating | Symbol | Min | Typ | Max | Units |
| Input capacitance | C_{IN} | | | 7 | pF |
| CMR ratio | | 40 | | | dB |
| Open loop gain (DC) | | 40 | | | dB |
| Gain Bandwidth product (20dB/decade roll off) | | 1 | 5 | | MHz |
| OUTPUT: OA3 | | | | | |
| Output voltage low at $I_{OL} = -1mA$ | V_{OL} | 0 | | 1 | V |
| Output voltage high at $I_{OH} = 1mA$ | V_{OH} | 8 | | VDD2 +0.5 | V |
| VCO AMPLIFIER VC01, VC02 | | | | | |
| Mutual conductance at 100KHz | See gm | 1.5 | | | mA/V |
| Bandwidth (-3dB cut off frequency) | Fig 9 Bgm | 20 | | | MHz |
| Input capacitance | C_{IN} | | | 7 | pF |
| Output capacitance | C_{OUT} | | | 7 | pF |
| Feedback capacitance | C_{FB} | | | 5 | pF |
| Input leakage | (1) I_{IN} | -1 | | +1 | μA |
| Output current (at 10MHz) | I_{out} | -1 | | +1 | mA |
| Small signal voltage gain at 100KHz | See A_V | 4 | | | V/V |
| TIMING | | | | | |
| Operating frequency (except VCO) | F_{cfm} | 0.1 | | 5 | MHz |
| Operating frequency (VCO only) | F_{vco} | 0.2 | | 10 | MHz |
| OUTPUTS: CLDE, DADE, SSDE, FSDE, CEFM (see Figure 5) | (6,12) | | | | |
| Output rise time | t_{OR} | | | 50 | ns |
| Output fall time | t_{OF} | | | 40 | ns |
| CLDE period | t_{OCP} | 400 | | | ns |
| CLDE high time | t_{OCH} | 150 | | | ns |
| CLDE low time | t_{OCL} | 150 | | | ns |
| DADE/SSDE/FSDE to CLDE set up | t_{ODS} | 100 | | | ns |
| CLDE to DADE/SSDE/FSDE hold | t_{ODH} | 100 | | | ns |
| SSDE low time | (7) t_{SSL} | | | 3 | CEFM period |
| CLDE low time during FSDE | (8) t_{OCG} | | | 46 | CEFM period |
| CLDE to CEFM set up | t_{ODSE} | 16 | | 100 | CEFM period |
| CEFM to CLDE hold | t_{ODHE} | | | 100 | CEFM period |

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| ISSUED BY: D. Braithwaite | 9 SH SH 15 | 3.2.82 | 13.7.82 |
| | | 14.4.83 | |

| Electrical Characteristics | Operating - timing | Unit | Symbol | Value | | |
|--|---|----------------|-------------------|-------|-----|------|
| | | | | Min | Typ | Max |
| <u>OUTPUTS:</u> SECL, SDATA, P, SWCL (see Figure 6) | | (12,13, 14) | | | | |
| | Output rise time (SECL, SDATA) | (6) | t _{OR} | | 50 | ns |
| | Output fall time (SECL, SDATA) | (6) | t _{OF} | | 40 | ns |
| | Output rise time (P, SWCL) | (9) | t _{OSR} | | 200 | ns |
| | Output fall time (P, SWCL) | (9) | t _{OSF} | | 200 | ns |
| | SECL high time | | t _{OCH} | 150 | | ns |
| | SECL low time | | t _{OCL} | 150 | | ns |
| | SDATA to SECL set up | | t _{ODS} | 100 | | ns |
| | P to SWCL set up | | t _{ODSP} | 1 | | µs |
| | SECL to SDATA hold | | t _{ODH} | 100 | | ns |
| | SECL to SWCL hold | | t _{SWH} | 0 | 500 | ns |
| | SWCL Duty cycle (t _{high} /t _{period}) | | | 40 | 50 | 60 % |
| <u>OUTPUT:</u> FD | | (12) | | | | |
| | Output rise time | (6) | t _{FDR} | | 1 | µs |
| | Output fall time | (6) | t _{FDF} | | 1 | µs |
| <u>OUTPUTS:</u> DEFM, <u>CEFM</u> (see Figure 7) | | (6,12) | | | | |
| | Output rise time | | t _{OR} | | 50 | ns |
| | Output fall time | | t _{OF} | | 40 | ns |
| | DEFM to <u>CEFM</u> set up | (18) | t _{ODS} | 50 | | ns |
| | <u>CEFM</u> to DEFM hold | (18) | t _{ODH} | 70 | | ns |
| | <u>CEFM</u> high time | | t _{OCH} | 50 | | ns |
| | <u>CEFM</u> low time | | t _{OCL} | 50 | | ns |

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NOTES

1. Vin = 0.3 to 6.0V, 25°C, measured with VDD1 = 6.0V
2. short circuit protected to VDD1 and VSS. The maximum load capacitance that can be applied before short circuit protection becomes operative is 150pF.
3. output in high impedance state 25°C.
4. 25°C
5. all tests done within common mode voltage range
6. output loading 50pF
7. SSDE remains low for only one negative edge of CLDE
8. excessive bit-slip may cause gap to disappear
9. output loading 150pF
10. the SYNC bit is low when a subcoding sync word is detected.
11. CLDE remains low when FSDE is high
12. reference levels are 0.8V and 2.4V
13. output loading 50pF for SECL and SDATA, and 150pF for SWCL and P
14. SWCL has a 50% duty cycle.
15. Average data run length = 5x CEFM periods
16. 100kΩ connected between output and VSS, VDD1 = 5V
17. 100kΩ connected between output and VDD1, VDD1 = 5V
18. Free running VCO frequency tuned to nominal & PLL in lock with a typical application circuit is shown in Figure 1.
19. Measured with Viac = 1v p-p undistorted EFM signal

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REVISIONS: 1. 10/11/81
 2. 11/11/81
 3. 12/11/81
 4. 13/11/81
 5. 14/11/81
 6. 15/11/81
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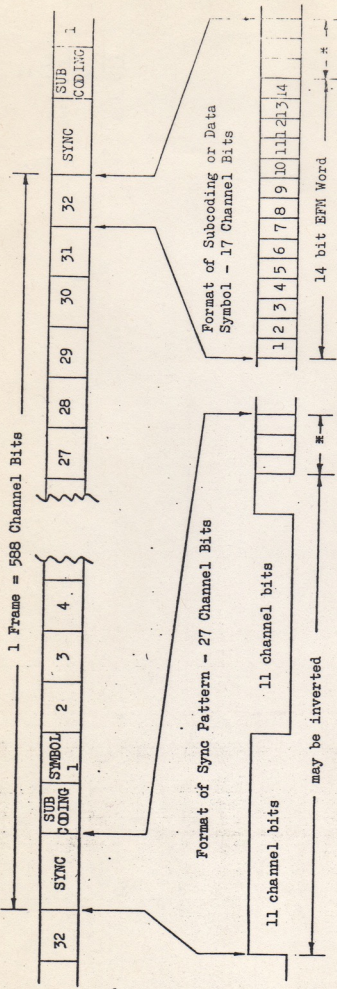


FIGURE 2 - HF Input Waveform

| | | | |
|---------------------------------------|--------------------------------|--------|-----------------|
| FUNCTION: Compact Disc Demodulator | COMM: SAA 7010 EXP: M4290 A | DATE | 08.01.82 |
| | | 3.2.82 | 13.7.87 |
| ISSUED BY: D. Braithwaite | 13 SH SH | 19 | 23.2.82 14.4.83 |

FIGURE 3 - Output Waveforms (To ERCO)

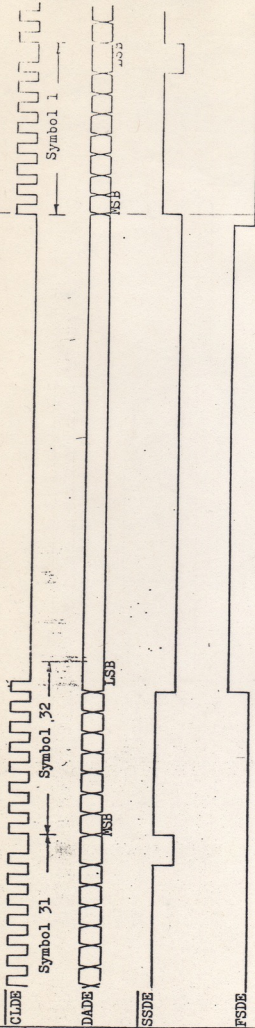
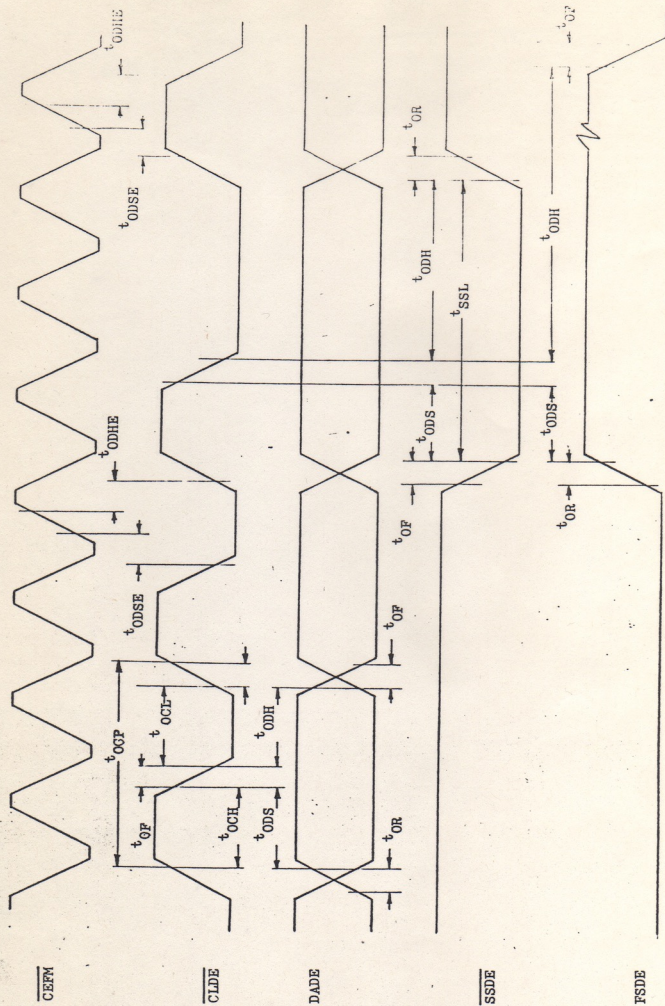


FIGURE 4 - Output Waveforms (Subcoding)



| | | | | |
|---------------------------|--|----------------|---------|----------|
| FUNCTION: | | COMM: SAA 7010 | DATE | 08.03.82 |
| Compact Disc Demodulator | | EXP: M4290A | 3.2.82 | 13.7.82 |
| ISSUED BY: D. Braithwaite | | 14 SH/SF | 23.2.82 | 14.4.83 |
| | | | | |

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 ORIGINAL AUTHOR OR PUBLISHER



See notes (6), (12)

Figure 5. Output Waveform Timing (to ERCO)

| | | | |
|------------------------------------|--|-----------------------|-----------------|
| FUNCTION: Compact Disc Demodulator | | COMM: SAA7010 M4290 A | DATE: 08.03.82 |
| ISSUED BY: D. Braithwaite | | EXP: 15 SH/SH 19 | 14.4.83 13.7.82 |

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 PARTIES IN ANY FORM WHATEVER

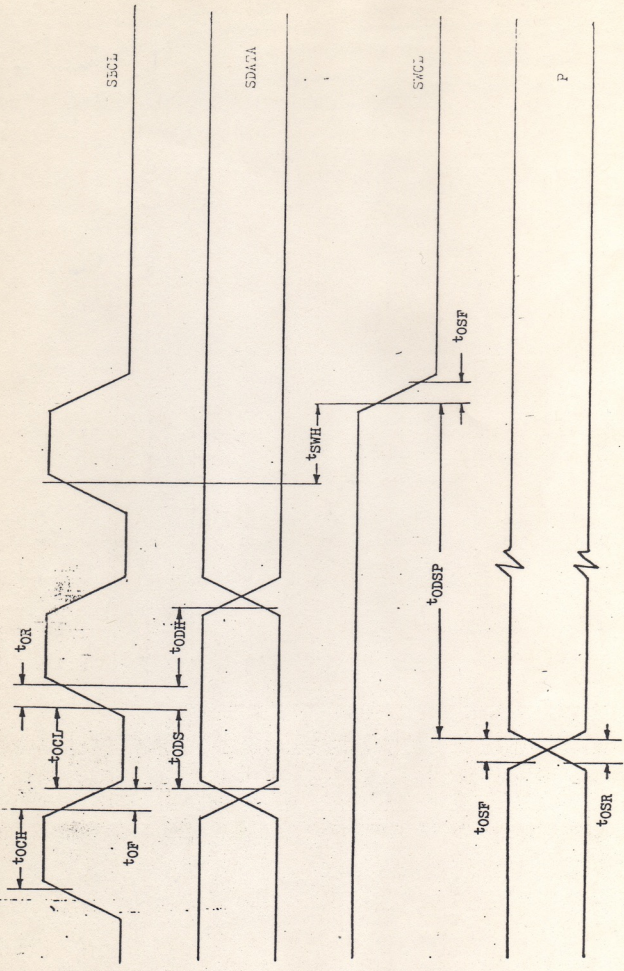


FIGURE 6 - Output Waveform Timing (Sub Coding)

see Notes 12, 13 and 14

| | | | |
|---------------------------|----------------|---------|----------|
| FUNCTION: | COMM: SAA 7010 | DATE | 08.03.82 |
| Compact Disc Demodulator | EXP: M4290 A | 3.2.82 | 13.7.82 |
| ISSUED BY: D. Braithwaite | 16 SH SH 19 | 23.2.82 | 14.4.83 |

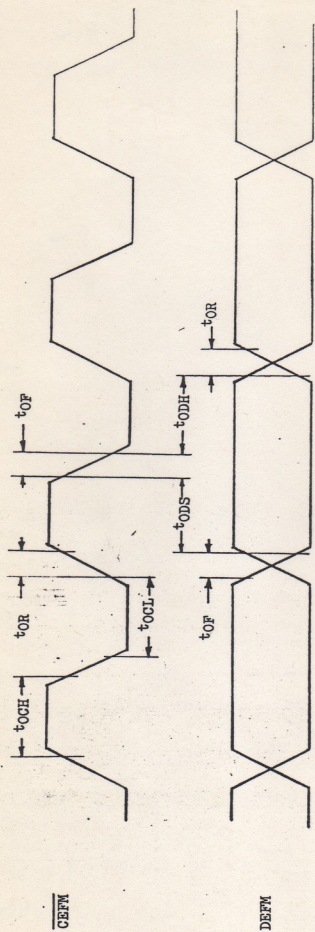


FIGURE 7 - Output Waveform Timing (EFM outputs)

see notes 6, 12

REPLACES SAA 7010
 DESIGN OF SAA 7010 IS NOT TO BE
 CHANGED WITHOUT THE APPROVAL OF
 PHILIPS

FUNCTION:

Compact Disc Demodulator

COMM: SAA 7010

EXP: M4290 A

DATE

23.2.82

08.03.82

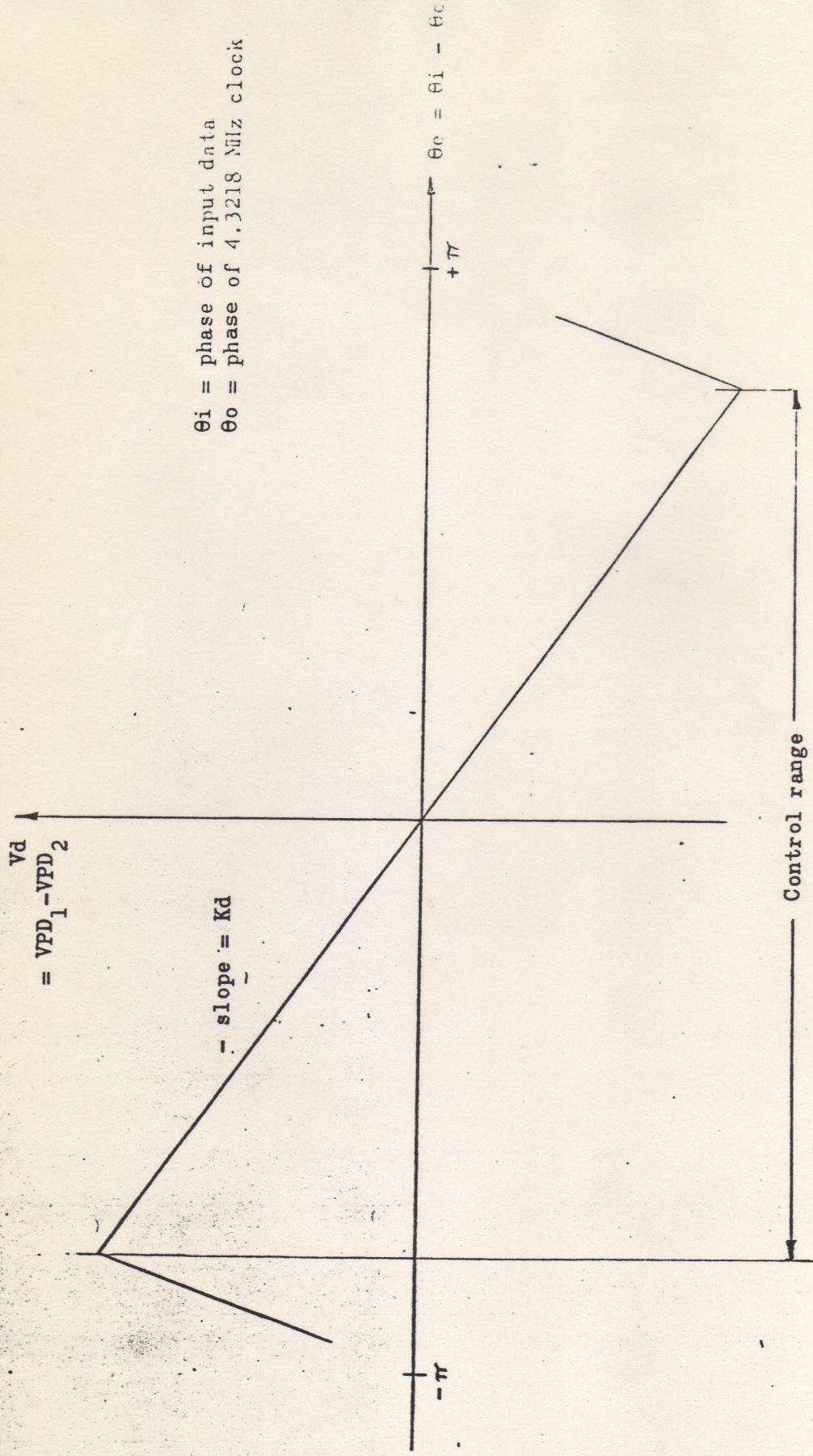
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ISSUED BY: D. Braithwaite

17 SH | SH 19

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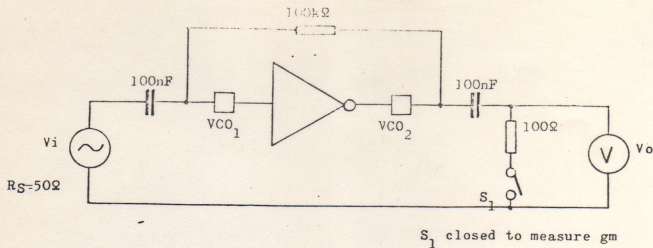
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θ_i = phase of input data
 θ_o = phase of 4.3218 MHz clock

Figure 8 Typical Phase Detector Characteristic

| | | | |
|-----------------------------|------------------------------------|---------------|-----------------|
| | FUNCTION: Compact Disc Demodulator | COMM: SAA7010 | DATE |
| | ISSUED BY: D. Braithwaite | EXP: M4290 A | 8.03.82 14.4.83 |
| | | 18 SH SH 19 | 13.7.82 |
| MULLARD LIMITED SOUTHAMPTON | | | |

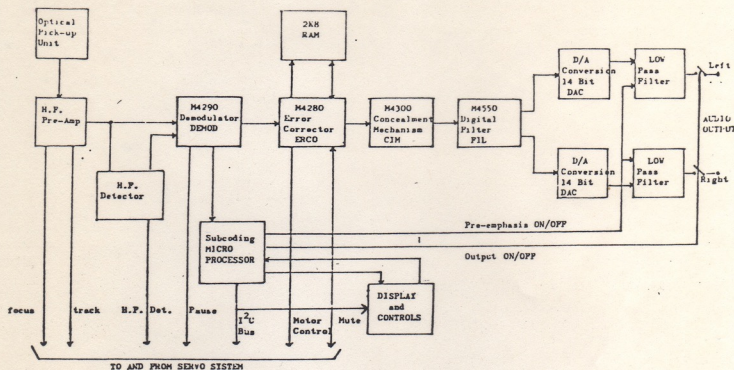


$$g_m = \frac{I_o}{V_i} = \frac{10 \times V_o}{V_i} \quad \text{mA/V}$$

Figure 9. Measurement circuit for VCO voltage gain and gm

| | | | | |
|------------------------------------|--|---------------|---------|---------|
| FUNCTION: Compact Disc Demodulator | | COMM: SAA7010 | DATE | |
| ISSUED BY: D. Braithwaite | | EXP: M4290 A | 8.03.82 | 14 4 83 |
| 19 SH SH 19 | | 13.7.82 | | |
| MULLARD LIMITED SOUTHAMPTON | | | | |

Simplified Block Diagram for the Compact Disc Digital Audio System

SYSTEM DESCRIPTION

The information contained in the pit structures on the disc is converted to a coded input signal via the Optical Pick-up Unit. This signal is amplified and filtered to remove the low frequency tracking information and to equalise the frequency response.

The M4290 DEMOD re-generates the data rate bit clock and timing signals from the H.F. input signal. This EFM modulated signal is decoded into a N.R.Z. form and the subcoding data extracted and fed to the external Subcoding Microprocessor. The decoded 8 bit data symbols are fed serially into the Error Corrector I.C. together with timing signals.

| | | | |
|--|---------------------|-----------|----------|
| | FUNCTION: | COM: | DATE |
| | Compact Disc System | EXP: | 19.11.81 |
| | ISSUED BY: D. Noble | 1 SH SH 2 | |

The M4280 ERCO corrects up to two erroneous symbols per frame in the data received from DEMOD. The necessary de-interleaving to obtain the required data format is achieved by writing out the data in 8 bit parallel symbols to an external RAM and then reading it back in a defined sequence. After all possible corrections have been made the data is fed out of ERCO in a 16 bit serial format. A further function of ERCO is to re-synchronise the data to a steady 2.1166MHz clock rate derived from a 4.2336MHz crystal oscillator on the CIM I.C. This removes any jitter from the data while further operations eliminate wow and flutter plus any F.M. content in the data signal. If the ERCO is unable to correct error bits then the uncorrected data is passed to CIM together with an Unreliable Data warning signal.

The M4300 CIM accepts the 16 bit serial data and acts in such a way that, if the Unreliable Data signal is received, the effect of the errors is minimised. If the error results in a single unreliable sample then this is interpolated by replacing it by a new sample whose value is calculated from the values of the good sample immediately preceding it and that succeeding it. If a string of unreliable samples is received then the output is muted by replacing unreliable samples with zero value samples and reducing the value of the thirty samples preceding and succeeding them to smooth out the effects of the transition. The output of CIM is split into fourteen or sixteen bit stereo left or right data in Offset Binary or Twos Complement format.

The M4550 FIL is a digital interpolating filter which improves the signal to noise ratio. It also enables a simpler analogue filter to be used after the Digital to Analogue Converter (DAC). The M4550 is a low pass digital transversal filter with 96 taps. The stereo output is organised in serial fourteen bit samples with the M.S.B. first. It is switchable between Offset Binary and Twos Complement code. The output sample frequency is 176.4KHz which is four times the input sampling frequency.

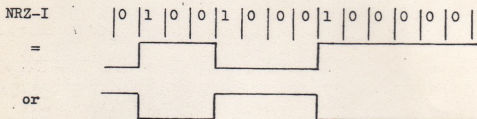
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| | | FUNCTION: Compact Disc System | CONN: | DATE 19.11.81 | |
| | | ISSUED BY: D. Noble | 2 SH 2 | | |

EFM Decoding System

The Eight to Fourteen Modulation (EFM) code used in the Compact Disc Digital Audio system is designed to restrict the bandwidth of the data on the disc and present a d.c. free signal to the demodulator. The actual number of bits per symbol is 17 which includes 3 merging bits which also help to remove the d.c. content.

Table 1 shows the conversion from 8 bit NRZ symbols to the equivalent 14 bit symbols. The 14 bit symbols are given in NRZ-I representation in which a 1 means a transition at the beginning of that bit from high-low or low to high i.e.



C1 is the first bit of the 14 bit symbol read from the disc and D1 is the Most Significant Bit (MSB) of data which appears first at the DADE output from DEMOD.

The codes shown in Table 1 cover the normal 256 possibilities for an 8 bit data word. However, there are several other combinations of 14 bit codes which, although they obey the EFM rules for maximum and minimum run length, will produce unspecified output data symbols. Two of these extra codes are used in the subcoding data to define a subcoding frame sync.

These are:-

| D1 | D8 | C1 | C14 |
|--------------------|----|-----------------------------|-----|
| 1 1 1 1 1 0 0 0 | | 0 0 1 0 0 0 0 0 0 0 0 0 0 1 | |
| 1 0 1 1 1 1 1 0 | | 0 0 0 0 0 0 0 0 0 1 0 0 1 0 | |
| W V U T S R Q SYNC | | | |

When a subcoding frame sync is detected the P bit of the data is ignored by the debounce circuitry. The remaining bits Q - W are not specified in the system but will always be as shown from this device.

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| FUNCTION: | COMM: SAA 7010 | DATE | |
| Compact Disc Demodulator | EXP: M4290 | 3.2.82 | |
| ISSUED BY: D. Braithwaite | 1 SH SH 2 | | |