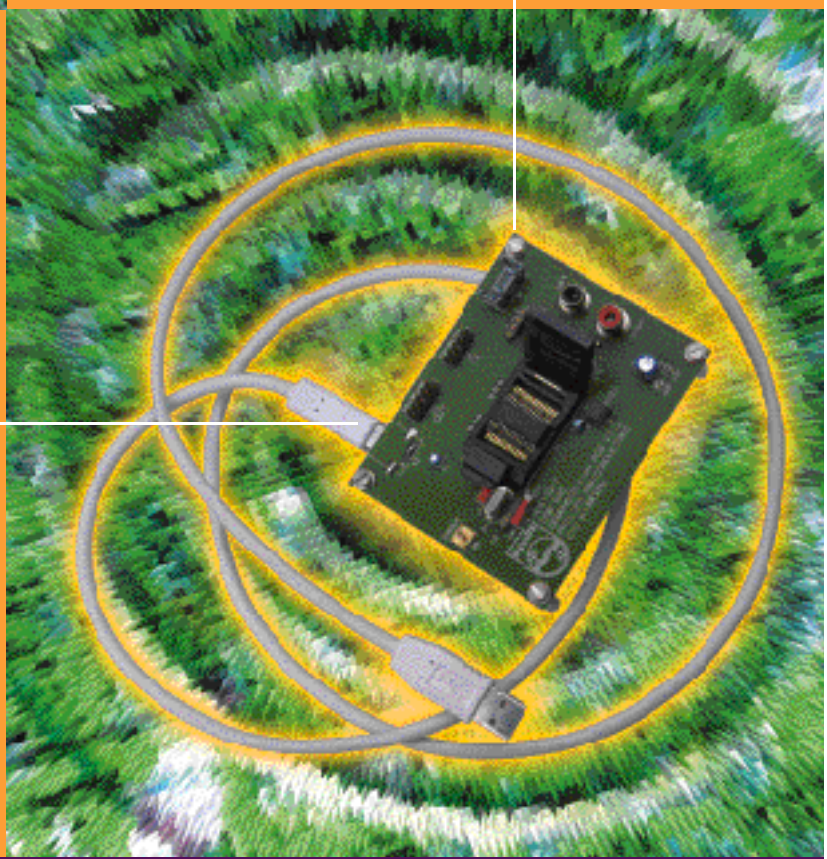
Semiconductors for Digital Audio



designer's guide August 1997

Philips Semiconductors

Contents

NOTE
Purchase of Philips I²C components conveys a license under the Philips I²C patent to use the components in the I²C system, provided the system conforms to the I²C specifications defined by Philips.

INTRODUCTION

PHILIPS' IC SOLUTIONS FOR DIGITAL AUDIO CONVERSION AND PROCESSING

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This guide supplements Data Handbook IC01 (Semiconductors for Radio and Audio systems) to provide a simple means of evaluating the features and performance of the extensive range of Philips' audio data converters and dedicated signal processing ICs.

Digital audio data converters

Philips scored a first in 1987 by developing the bitstream data conversion technique which converts binary samples of an analog audio signal into a 1-bit code using oversampling, noise shaping and pulse density modulation (PDM). Compared with multi-bit DACs, our bitstream conversion DACs have improved small-signal linearity, no "glitches" and no crossover distortion effects. We have a wide range of DACs of this type plus digital filters for, noise shaping, digital filtering and post filtering requirements of all classes of digital audio equipment.

We also have a wide selection of conventional 16-bit DACs and a quadruple sign-magnitude filter DAC (QDAC) for front and rear stereo in car applications. Our range of audio data convertors s is completed with four bitstream ADCs and a range of advanced CODECs.

MPEG decoders

As one of the members of MPEG, Philips is playing an active role in developing and refining MPEG compression standards. The depth of Philips expertise is reflected in the quality of its MPEG ICs, which implement the standards in full, delivering excellent decompression audio quality. Philips has a family of dedicated audio MPEG-1 and MPEG-2 decoders including a version for decoding MPEG II 7.1, 5.1 and 2 channels.

Other important dedicated Philips products for digital audio systems include a digital input/output circuit (DAIO), a general digital input circuit (GDIN), a digital audio processing IC (DAPIC), and a headphone driver.

Data transfer in digital audio systems

Exchanging audio data between ICs in a digital audio system is often hampered because each manufacturer incorporates his own dedicated interface. This makes it difficult to use ICs from different manufacturers in the same system. For maximum design flexibility, a vital requirement for both the equipment manufacturer and the IC manufacturer is the availability of standardized communication structures. To meet this requirement, Philips developed the Inter-IC Sound (I^2S) interface.

The I^2S-interface

The I^2S-interface is a serial link dedicated to data transfer between ICs in digital audio systems. Signals other than audio data, such as sub-coding and control, are transferred separately. To minimize the number of pins, and to keep the wiring simple, I^2S is a serial interface consisting of 3 lines; serial data (SD) for two time-division multiplexed channels, left/right channel word select (WS), and serial clock (SCL).

The transmitter and receiver have the same clock signal for data transmission. In a simple two-IC system, the master (transmitter or receiver), must generate the bit clock and word select signal, and the transmitter generates the data.

Customer support

Naturally, Philips Semiconductors support for digital audio data converters and dedicated signal processing ICs doesn't end with the supply of this extensive range of ICs described in this guide. We also offer access to the wide-ranging expertise of our international system laboratories to assist with your hardware/software designs for specific applications. Should you require further information, please contact your nearest Philips National Organisation – you'll find their addresses on the back cover of this guide.

INTRODUCTION

Review of ICs

DIGITAL AUDIO DATA CONVERTERS

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Essential functions in digital audio equipment are the analog-to-digital conversion (ADC), and the digital-to-analog conversion (DAC). These signal processing stages play a major and critical role by converting audio signals into 16-bit sound data words (ADC), and by converting 16-bit sound data words which have been numerically decoded and filtered, into analog waveforms which can be made audible (DAC)

Philips has developed an extensive range of stereo data converters using several different conversion techniques to meet the diverse requirements of the digital audio market:

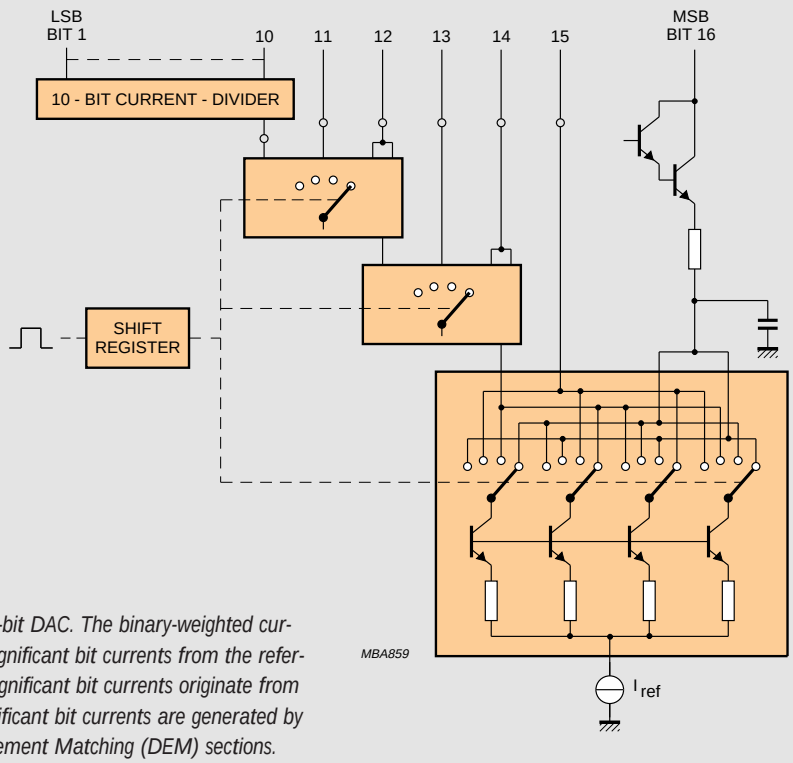
- Standard 16-bit stereo DACs
- Bitstream conversion stereo ADCs and DACs for top-class audio performance
- Continuous calibration stereo DACs which are the world's smallest converters with the lowest power consumption
- Stereo filter-DACs that use bitstream conversion for small signals, and the continuous calibration technique for large signals
- A quadruple sign-magnitude filter-DAC for 4-channel (front and rear stereo) digital audio applications in cars
- Bitstream conversion ADCs
- Combined stereo bitstream ADCs with digital filter and bitstream/continuous calibration DACs
- Universal Serial Bus (USB) DAC and CODEC for USB-compliant audio and multimedia applications.

Standard 16-bit DACs

With these DACs, the ten lowest bits are derived from a reference current by means of a passive 10-bit current divider based on emitter scaling. The six highest bits are constructed by dynamic element matching (DEM), a technique patented by Philips.

As shown in the figure below, DEM uses matched resistors to divide a reference input current into four nearly equal parts. Under control of an internal shift register, the four currents are interchanged with a frequency of 250 kHz from an internal oscillator. After time-averaging, the resulting four output currents are very closely matched.

Two of the four output currents generated in the first DEM stage are added to form the largest (MSB = bit 16) bit current. The third output current forms the second largest (MSB – 1 = bit 15) bit current. The fourth output current is fed into the next DEM stage to construct bits 13 and 14. Similarly, the fourth output current from the second DEM stage is fed into the final DEM stage to construct bits 11 and 12. The fourth output current from the final DEM stage is fed to the passive 10-bit current divider to construct the 10 LSBs (bits 1 to 10). In this manner, all sixteen bit currents are derived from the same current reference.



Structure of a high-performance 16-bit DAC. The binary-weighted current network derives the 16 most-significant bit currents from the reference current source. The 10 least-significant bit currents originate from the passive divider. The 6 most-significant bit currents are generated by time-averaging in the 3 Dynamic Element Matching (DEM) sections.

The bitstream conversion technique

The bitstream digital-to-analog conversion technique, developed by Philips, converts binary samples (e.g. 16-bit words) into a 1-bit code representing two levels (0 or 1) using oversampling, noise shaping and pulse density modulation (PDM). This code is then converted into an analog form that closely resembles the original signal by a switched-capacitor conversion technique. Because bitstream converters process the signal in the digital domain, they have the following advantages over conventional multi-bit converters:

- Considerable improvement of small-signal linearity
- Absence of glitches
- Complete elimination of cross-over effects.

Continuous calibration DACs (CC-DACs)

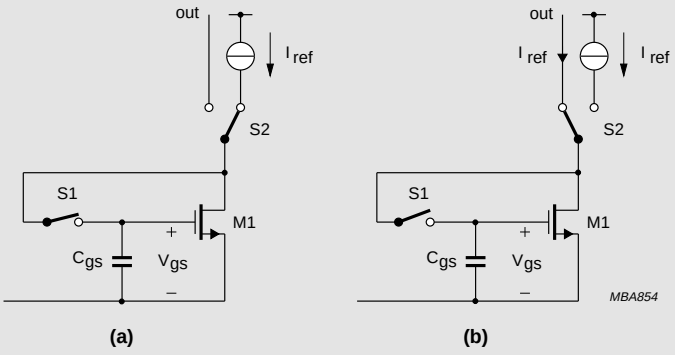
Continuous calibration is an innovative data conversion technique patented by Philips and implemented in our new range of CMOS CC-DACs for cost-effective D to A conversion in portable equipment.

The technique of continuous calibration is based on the principle of storing charges on the gate-source capacitance of internal CMOS transistors. This charge storage principle allows the largest bit currents to be generated repeatedly from a single reference current. Because only one internal reference source is required, these coarse bit currents are extremely closely matched and immune to ageing, temperature and process variations or matching.

The basic operation of a CC-DAC (see figure below) consists of continuous cycles of calibrating the drain current of CMOS transistors to a reference current, and then extracting an exact duplicate of the reference current from the drain. During calibration, the MOS transistor is connected as a diode in parallel with its gate-source capacitance by linking its drain and gate. The drain of this diode-connected transistor is connected to a constant reference current source so that the intrinsic gate-source capacitance charges to a voltage determined by the characteristics of the transistor. The drain-gate link and reference current source are then disconnected and, since the charge on the intrinsic gate-source capacitance of the transistor is preserved, an exact duplicate of the reference current is available as an output at the drain.

CC-DACs use symmetrical offset decoding in which the bit switching is arranged so that the zero-crossing transition is performed by switching only the smallest currents. The intrinsic highly accurate coarse current, combined with the symmetrical offset principle, precludes any distortion at the zero-crossing or at any other small-signal transitions. CC-DACs are therefore capable of high-quality reproduction of low-level audio input signals.

Philips' CC-DACs are fabricated in a 1.0 µm CMOS process and feature extremely low power dissipation, small packages and simple application.



Principle of continuous calibration (a) calibration (b) operation.

Main application areas of digital audio converters

Type	Description	Home hi-fi	Portable hi-fi	Car	Multimedia
SAA7360GP	high-performance bitstream ADC	✓		✓	
SAA7366T	economy bitstream ADC	✓		✓	
SAA7367T	economy bitstream ADC	✓		✓	
TDA1305T(AT)	bitstream/CC filter-DAC	✓	✓	✓	✓
TDA1306T	CC filter-DAC	✓	✓	✓	✓
TDA1307	high-performance bitstream digital filter	✓			
TDA1309H	low-voltage bitstream/CC ADC + DAC	✓	✓	✓	
TDA1310A(AT)	continuous calibration DAC with current output	✓	✓	✓	✓
TDA1311A(AT)	continuous calibration DAC with voltage output	✓	✓	✓	✓
TDA1312A(AT)	continuous calibration DAC with voltage output	✓	✓	✓	
TDA1313(T)	continuous calibration DAC with voltage output	✓	✓	✓	
TDA1314T	quad sign-magnitude filter-DAC with voltage output	✓	✓	✓	
TDA1386T	CC filter-DAC	✓	✓	✓	
TDA1387T	continuous calibration DAC with current output	✓	✓	✓	✓
TDA1388T	bitstream/CC filter DAC	✓			✓
TDA1541A	high-performance 16-bit DAC	✓			
TDA1541A/R1	high-performance 16-bit DAC	✓			
TDA1541A/S1	single crown 16-bit DAC	✓			
TDA1541A/S2	double crown 16-bit DAC	✓			
TDA1543(T)	economy 16-bit DAC	✓		✓	
TDA1545A(AT)	continuous calibration DAC with current output	✓	✓	✓	
TDA1547	top-grade BiMOS bitstream DAC	✓			
TDA1548T	low-voltage bitstream/CC filter-DAC with DSP features		✓	✓	
TDA1549(T)	bitstream/CC DAC	✓	✓	✓	
UDA1309H	low-power stereo bitstream DAC	✓			
UDA1320TZ	low-voltage bitsream filter DAC		✓	✓	
UDA1321	USB DAC				✓
UDA1322TS	low-voltage bitstream DAC with DSP features		✓		
UDA1324TS	ultra low-voltage bitstream filter DAC		✓		
UDA1325	USB ADC/DAC				✓
UDA1340M	low-voltage stereo filter ADC/DAC with DSP	✓	✓		
UDA1341TS	low-voltage stereo filter ADC/DAC with DSP	✓	✓		

Survey of stereo audio converters in type number sequence

Type	Description		Over-sampling (x f_s)	Data format	Typ. THD + N at 0 dB dB(%)	Typ. THD + N at -60 dB [4] dB(%)	Typ. SNR [4] (dB)	Typ. output voltage (or current) [6] V (mA)	Supply voltage (V)	Power dissipation (mW)	Package
SAA7360GP	high-performance bitstream ADC		128	data output format: I^2S + two pseudo I^2S	-90(0.003)		102		5 ±10%	410	QFP44
SAA7366T	economy bitstream ADC		128	data output format: I^2S + one pseudo I^2S	-88(0.004)		95		5 ±10%	350	SO24
SAA7367T	economy bitstream ADC		128	data output format: I^2S + one pseudo I^2S	-88(0.004)		95		5 ±10%	150	SO24
TDA1305T(AT)[2)6)]	bitstream/CC filter-DAC		96	I^2S, “S”, $1f_s$, up to 20-bit	-90(0.003)	-46(0.5)	108	1.5	3.4 to 5.5	70	SO28
TDA1306T[2)6)]	CC filter-DAC		4	I^2S, “S”, $1f_s$, up to 20-bit	-70(0.032)	-42(0.8)	108	1.1	5 ±10%	50	SO24
TDA1309H	low-voltage bitstream/CC ADC + DAC	**ADC**		I^2S, “S”, 16-, 18-bit output	-85(0.005)	-35(1.7)	95		2.7 to 4.0	72	QFP44
		DAC	256	I^2S, “S”, 16-, 18-bit input	-90(0.003)	-44(0.6)	104	0.5		84	
TDA1310A(AT)	continuous calibration DAC with current output		1	“S”, up to $4f_s$	-65(0.05)	-33(2.2)	95	(1.0)	3 to 5.5	6	DIL8, SO8
TDA1311A(AT)[5)]	continuous calibration DAC with voltage output		1	“S”, up to $4f_s$	-68(0.04)	-33(2)	92	2.0	4 to 5.5	17	DIL8, SO8
TDA1312A(AT)[5)]	continuous calibration DAC with voltage output		1	“S”, up to $8f_s$	-68(0.04)	-33(2)	92	2.0	4 to 5.5	17	DIL8, SO8
TDA1313(T)[5)]	continuous calibration DAC with voltage output		1	“S”, up to $8f_s$	-88(0.004)	-38(1.3)	98	4.2	3 to 5.5	15	DIL16, SO16
TDA1314T[5)]	quad sign-magnitude filter-DAC with voltage output		4	2 x I^2S, $1f_s$, 18-bit with sign	-70(0.03)	-42(0.8)	110	2.0	5 ±5%	85	SO28
TDA1386T[2)]	CC filter-DAC		4	I^2S, “S”, $1f_s$, up to 20-bit	-70(0.032)	-42(0.8)	108	1.1	5 ±10%	50	SO24
TDA1387T	continuous calibration DAC with current output		1	I^2S, up to $4f_s$	-88(0.004)	-35(1.7)	98	(1.0)	3 to 5.5	28	SO8
TDA1388	bitstream/CC filter-DAC for CD-ROM		96	I^2S, “S”, $1f_s$, up to 20-bit	-85(0.005)	-35(1.7)	100	0.8	2.7 to 3.6	24	SSOP16
TDA1541A[3)]	high-performance 16-bit DAC		1	I^2S, up to $8f_s$	-95(0.0018)	-42(0.79)	112	(4.0)	5 ±10%	700	DIL28
TDA1541A/R1[3)]	high-performance 16-bit DAC		1	I^2S, up to $8f_s$	-95(0.0018)	-43(0.7)	112	(4.0)	5 ±10%	700	DIL28
TDA1541A/S1[3)]	single crown 16-bit DAC		1	I^2S, up to $8f_s$	-95(0.001)	-47(0.4)	112	(4.0)	5 ±10%	700	DIL28
TDA1541A/S2[3)]	double crown 16-bit DAC		1	I^2S, up to $8f_s$	-97(0.002)	-47(0.4)	112	(4.0)	5 ±10%	700	DIL28
TDA1543(T)	economy 16-bit DAC		1	I^2S, up to $4f_s$	-75(0.018)	-33(2.2)	96	(2.30)	3 to 8	250	DIL8, SO16
TDA1545A(AT)	continuous calibration DAC with current output		1	“S”, up to $4f_s$	-88(0.004)	-35(1.7)	101	(1.0)	3 to 5.5	6	DIL8, SO8

continued on page 2-6

Survey of stereo audio converters in type number sequence (continued)

Type	Description		Over-sampling (x f_s)	Data format	Typ. THD + N at 0 dB dB(%)	Typ. THD + N at -60 dB [4] dB(%)	Typ. SNR [4] (dB)	Typ. output voltage (or current) [6] V (mA)	Supply voltage (V)	Power dissipation (mW)	Package
TDA1547[1]	top-grade BiMOS bitstream DAC		24	1-bit, 192f_s	-101(0.0009)	-51(0.02)	113	1.0	5 ±10%	800	DIL32
TDA1548T[2]	low-voltage bitstream/CC filter-DAC + DSP features		96	I^2S, “S”, 1f_s, up to 20-bit	-85(0.005)	-35(1.8)	95	0.7	2.7 to 4	50	SO28
TDA1549T [5]	bitstream/CC DAC		24	“S”, 4f_s, 18-bit	-90(0.003)	-50(0.32)	110	1.5	3.8 to 5.5	50	SO16
UDA1309H	low-voltage bitstream/CC ADC + DAC	**ADC**		I^2S, “S”, 16-, 18-bit output	-85(0.005)	-35(1.7)	95		4.5 to 5.5	140	QFP44
		DAC	256	I^2S, “S”, 16-, 18-bit input	-90(0.003)	-44(0.6)	104	1.0		120	
UDA1320TZ	low-voltage bitstream filter DAC		128	I^2S, “S”, up to 20-bit	-85(0.005)	-35(1.7)	100	0.8	2.7 to 3.6	24	SSOP16
UDA1321	low-voltage stereo filter DAC with DSP		128	I^2S, “S”, up to 20-bit + USB	-85(0.005)	-30(3.0)	95	0.8	3.0 to 3.6	150	SO28, SDIL32
UDA1322TS	low-voltage bitstream DAC with DSP features		128	I^2S, “S”, up to 20-bit	-90	-35	100	0.8	2.7 to 3.6	24	SSOP16
UDA1324TS	ultra low-voltage bitstream DAC		128	I^2S, “S”, up to 20-bit	-80	-30	90	t.b.d.	1.8 to 3.6	t.b.d.	SSOP16
UDA1325	USB CODEC	**ADC**		I^2S, “S”, up to 20-bit, USB output	-80(0.01)	-30(3.2)	95		5.0 to 3.6	t.b.d.	SDIL42, QFP44
		DAC	128	I^2S, “S”, up to 20-bit, USB input	-85(0.0056)	-30(3.2)	95	0.66		t.b.d.	
UDA1340M	low-voltage bitstream/CC ADC/DAC with DSP	**ADC**		I^2S, “S”, 16-, 18-bit output	-85(0.005)	-35(1.7)	95		2.7 to 3.6	27	SSOP28
		DAC	128	I^2S, “S”, up to 20-bit input	-90(0.003)	-35(1.7)	100	0.8		33	
UDA1341TS	low-voltage bitstream/CC ADC + DAC with DSP	**ADC**		I^2S, “S”, 16-, 18-bit output	-90(0.003)	-40(0.001)	100		2.7 to 3.6	45	SSOP28
		DAC	128	I^2S, “S”, up to 20-bit input	-95(0.002)	-40(0.001)	102	0.8		33	

NOTES:

1. measured with SAA7350 and 20-bit input; 2. includes digital filter; 3. high sound quality: dynamic element matching (DEM);
4. A-weighting; 5. includes I/V converter; 6. full-scale rms value.

Survey of stereo audio DACs (ranked by typical THD + N at 0 dB performance per category)

Type	Description	Over-sampling (x f_s)	Data format	Typ. THD + N at 0 dB dB(%)	Typ. THD + N at -60 dB dB(%) [4]	Typ. SNR (dB) [4]	Typ. output voltage (or current) [6] V (mA)	Supply voltage (V)	Power dissipation (mW)	Package
Bitstream DAC										
TDA1547[1]	top-grade BiMOS bitstream DAC	24	1-bit, 192f_s	-101(0.0009)	-51(0.02)	113	1.0	5 ±10%	800	DIL32S
Bitstream/continuous calibration DACs										
TDA1549T [5]	bitstream/CC DAC	24	"S", 4f_s, 18-bit	-90(0.003)	-50(0.32)	110	1.5	3.4 to 5.5	35	SO16
16-bit DACs										
TDA1541A/S2[3]	double crown 16-bit DAC	1	I^2S, up to 8f_s	-95(0.002)	-47(0.4)	112	(4.0)	5 ±10%	700	DIL28
TDA1541A/S1[3]	single crown 16-bit DAC	1	I^2S, up to 8f_s	-95(0.001)	-47(0.4)	112	(4.0)	5 ±10%	700	DIL28
TDA1541A[3]	high-performance 16-bit DAC	1	I^2S, up to 8f_s	-95(0.0018)	-42(0.79)	112	(4.0)	5 ±10%	700	DIL28
TDA1541A/R1[3]	high-performance 16-bit DAC	1	I^2S, up to 8f_s	-95(0.001)	-43(0.79)	112	(4.0)	5 ±10%	700	DIL28
TDA1543(T)	economy 16-bit DAC	1	I^2S, up to 4f_s	-75(0.018)	-33(2.2)	96	(2.3)	3 to 8	250	DIL8, SO16
Continuous calibration DACs										
TDA1313(T)[5]	continuous calibration DAC with voltage output	1	"S", up to 8f_s	-88(0.004)	-38(1.3)	98	4.2	3 to 5.5	30	DIL16, SO16
TDA1545A(AT)	continuous calibration DAC with current output	1	"S", up to 4f_s	-88(0.004)	-35(1.7)	101	(1.0)	3 to 5.5	6	DIL8, SO8
TDA1387T	continuous calibration DAC with current output	1	I^2S, up to 4f_s	-88(0.004)	-35(1.7)	98	(1.0)	3 to 5.5	28	DIL8, SO8
TDA1312A(AT)[5]	continuous calibration DAC with voltage output	1	"S", up to 8f_s	-68(0.04)	-33(2)	92	2.0	4 to 5.5	8	DIL8, SO8
TDA1311A(AT)[5]	continuous calibration DAC with voltage output	1	"S", up to 4f_s	-68(0.04)	-33(2.2)	92	2.0	4 to 5.5	8	DIL8, SO8
TDA1310A(AT)	continuous calibration DAC with current output	1	"S", up to 4f_s	-65(0.05)	-33(2.2)	95	(1.0)	3 to 5.5	6	DIL8, SO8

NOTES:

1. measured with SAA7350 and 20-bit input; 2. includes digital filter; 3. high sound quality: dynamic element matching (DEM);
4. A-weighting; 5. includes I/V converter.

Survey of stereo audio filter-DACs (ranked by typical THD + N at 0 dB performance per category)

Type	Description	Over-sampling (x f_s)	Data format	Typ. THD + N at 0 dB dB(%)	Typ. THD + N at -60 dB dB(%) [4]	Typ.SNR (dB) [4]	Typ. output voltage (or current) [6] V (mA)	Supply voltage (V)	Power dissipation (mW)	Package
Bitstream/continuous calibration filter-DACs										
TDA1305T(AT)[2)6)]	bitstream/CC filter-DAC	96	I^2S, “S”, $1f_s$, up to 20-bit	-90(0.003)	-46(0.5)	108	1.5	3.4 to 5.5	70	SO28
TDA1388	bitstream/CC filter-DAC for CD-ROM	96	I^2S, “S”, $1f_s$, up to 20-bit	-85(0.005)	-35(1.7)	95	1.0	4.5 to 5.5	110	SSOP28
TDA1548T[2)]	low-voltage bitstream/CC filter-DAC + DSP features	96	I^2S, “S”, $1f_s$, up to 20-bit	-85(0.005)	-35(1.8)	95	0.7	2.7 to 4	50	SO28
Continuous calibration filter-DACs										
TDA1306T[2)6)]	CC filter-DAC	4	I^2S, “S”, $1f_s$, up to 20-bit	-70(0.032)	-42(0.8)	108	1.1	5 ±10%	85	SO24
TDA1386T[2)]	CC filter-DAC	4	I^2S, “S”, $1f_s$, up to 20-bit	-70(0.032)	-42(0.8)	108	2.0	5 ±10%	50	SO24
Quadruple sign-magnitude filter-DAC										
TDA1314T[5)]	quad sign-magnitude filter-DAC with voltage output	4	2 x I^2S, $1f_s$, 18-bit with sign	-70(0.03)	-42(0.8)	110	2.0	5 ±5%	85	SO28
Bitstream filter-DACs										
UDA1322TS	low-voltage bitstream DAC with DSP features	128	I^2S, “S”, up to 20-bit	-90	-35	100	0.8	2.7 to 3.6	24	SSOP16
UDA1320TZ	low-voltage low-cost stereo filter DAC with DSP	128	I^2S, “S”, up to 20-bit	-85(0.005)	-35(1.7)	100	0.8	2.7 to 3.6	24	SSOP16
UDA1321	USB DAC	128	I^2S, “S”, up to 20-bit + USB	-85(0.005)	-30(3)	95	0.8	3.0 to 3.6	150	SO28, SDIP32
UDA1324TS	ultra low-voltage bitstream DAC	128	I^2S, “S”, up to 20-bit	-80	-30	90	t.b.d.	1.8 to 3.6	t.b.d.	SSOP16

NOTES:
1. measured with SAA7350 and 20-bit input; 2. includes digital filter; 3. high sound quality: dynamic element matching (DEM);
4. A-weighting; 5. includes I/V converter.

Survey of stereo audio ADCs (ranked by typical THD + N at 0 dB performance per category)

Type	Description	Over-sampling (x f_s)	Data format	Typ. THD + N at 0 dB dB(%)	Typ. THD + N at -60 dB dB(%) [4]	Typ. SNR (dB) [4]	Supply voltage (V)	Power dissipation (mW)
SAA7366T	economy bitstream ADC	128	I^2S + one pseudo I^2S	-88(0.004)		95	5 ±10%	350
SAA7367T	economy bitstream ADC	128	I^2S + one pseudo I^2S	-88(0.004)		95	5 ±10%	150
SAA7360GP	high-performance bitstream ADC	128	I^2S + two pseudo I^2S	-90(0.003)		102	5 ±10%	410

NOTES:
1. measured with SAA7350 and 20-bit input; 2. includes digital filter; 3. high sound quality: dynamic element matching (DEM);
4. A-weighting; 5. includes I/V converter.

Survey of stereo audio ADCs + DACs

Type	Description		Over-sampling (x f_s)	Data format	Typ. THD + N at 0 dB dB(%)	Typ. THD + N at -60 dB dB(%) [4]	Typ.SNR (dB) [4]	Typ. output voltage (or current) [6] V (mA)	Supply voltage (V)	Power dissipation (mW)	Package
TDA1309H	low-voltage bitstream/CC ADC/DAC	**ADC**		I^2S, “S”, 16-, 18-bit output	-85(0.005)	-35(1.7)	95		2.7 to 4.0	72	QFP44
		DAC	256	I^2S, “S”, 16-, 18-bit input	-90(0.003)	-44(0.6)	104	0.5		84	
UDA1309H	low-voltage bitstream/CC ADC/DAC	**ADC**		I^2S, “S”, 16-, 18-bit output	-85(0.005)	-35(1.7)	95		4.5 to 5.5	140	QFP44
		DAC	256	I^2S, “S”, 16-, 18-bit input	-90(0.003)	-44(0.6)	104	1.0		120	
UDA1325	USB CODEC	**ADC**		I^2S, “S”, up to 20-bit, USB output	-80(0.01)	-30(3.2)	95		3 to 3.6	t.b.d	SDIL42, QFP44
		DAC	128	I^2S, “S”, up to 20-bit, USB input	-85(0.0056)	-30(3.3)	95	0.66		t.b.d	
UDA1340M	low-voltage low-cost stereo filter ADC/DAC with DSP	**ADC**		I^2S, “S”, up to 20-bit output	-85(0.005)	-35(1.7)	95		2.7 to 3.6	27	SSOP28
		DAC	128	I^2S, “S”, up to 20-bit input	-95(0.002)	-35(1.7)	100	0.8		33	
UDA1341TS	low-voltage low-cost stereo filter ADC/DAC with DSP	**ADC**		I^2S, “S”, up to 20-bit output	-90(0.003)	-40(0.001)	100		2.7 to 3.6	45	SSOP28
		DAC	128	I^2S, “S”, up to 20-bit input	-95(0.002)	-40(0.001)	102	0.8		33	

UDA1320TZ/22TS/24TS

Bitstream filter DACs

UDA1320TZ

- **Low power, low voltage stereo DAC with integrated digital filter**
- **5 V tolerant inputs**
- **Control via static pins to provide enhanced functionality**
- **Selectable system clock frequencies (256 f_s and 512 f_s)**
- **Multiple format input interface compatible with I^2S-bus and LSB-justified**
- **Supports word lengths up to 20 bits (I^2S) and 16-, 18- and 20-bit (LSB)**
- **Digital de-emphasis for 44.1 kHz**
- **Soft mute**
- **High linearity, wide dynamic range, low distortion**
- **No analog post-filtering required**
- **Slave mode only applications**

UDA1322TS

All features of the UDA1320, plus:

- **Built-in DSP functions**
- **Control via L3 microcontroller interface**
- **Digital logarithmic volume and tone control**
- **Supports word lengths up to 20 bits (I^2S, MSB) and 16-, 18- and 20-bit (LSB)**
- **Selectable system clock frequencies (256 f_s, 384 f_s and 512 f_s)**
- **Digital de-emphasis for 32 kHz, 44.1 kHz and 48 kHz f_s**
- **Stereo line output under microcontroller volume control**

UDA1324TS

All features of the UDA1320, plus:

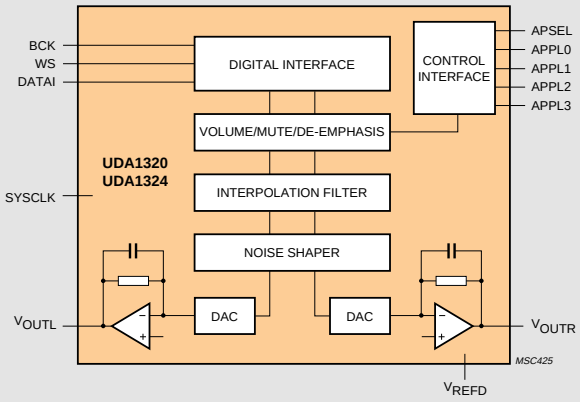
- **Control via L3 microcontroller interface**
- **Operates from a supply voltage as low as 1.8 V**
- **Supports word lengths up to 20 bits (I^2S, MSB) and 16-, 18- and 20-bit (LSB)**
- **Digital logarithmic volume control**
- **Digital de-emphasis for 32 kHz, 44.1 kHz and 48 kHz f_s**
- **Stereo line output under L3 volume control**

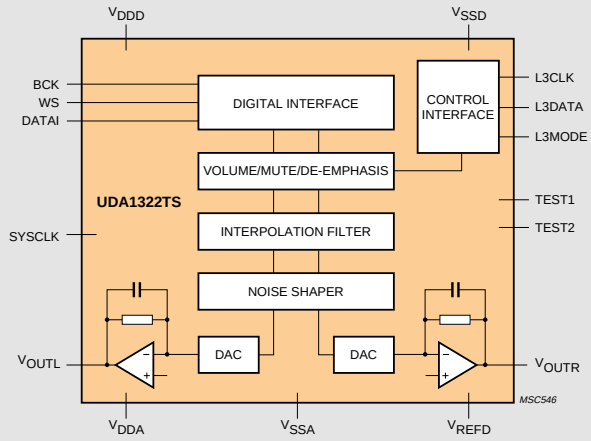
These single-chip stereo bitstream DACs operate from a low power supply and offer low power consumption, making them ideal for portable digital audio applications incorporating play-back functions.

The UDA1322TS offers full DSP features while the UDA1324TS is especially suited to operate at ultra-low supply voltages.

Both the UDA1322TS and the UDA1324TS are fully pin compatible with the UDA1320TZ.

QUICK REFERENCE DATA	UDA1320TZ	UDA1322TS	UDA1324TS
Supply voltage	2.4 to 3.6 V	2.7 to 3.6 V	1.8 to 3.6 V
Digital supply current	3 mA	3 mA	3 mA
DAC supply current	5 mA	6 mA	4 mA
Typical THD + N at 0 dB	–85 dB	–90 dB	–80 dB
Typical THD + N at –60 dB	–35 dB	–35 dB	–30 dB
SNR	100 dB	100 dB	90 dB
Package	SSOP16	SSOP16	SSOP16


BCK
WS
DATAI
DIGITAL INTERFACE
CONTROL INTERFACE
APSEL
APPL0
APPL1
APPL2
APPL3
VOLUME/MUTE/DE-EMPHASIS
UDA1320
UDA1324
SYSCLK
INTERPOLATION FILTER
NOISE SHAPER
DAC
DAC
VOUTL
VOUTR
MSC425
VREFD


VDDD
VSSD
BCK
WS
DATAI
DIGITAL INTERFACE
CONTROL INTERFACE
L3CLK
L3DATA
L3MODE
VOLUME/MUTE/DE-EMPHASIS
UDA1322TS
TEST1
TEST2
SYSCLK
INTERPOLATION FILTER
NOISE SHAPER
DAC
DAC
VOUTL
VOUTR
MSC546
VDDA
VSSA
VREFD

UDA1321

Bitstream filter DAC

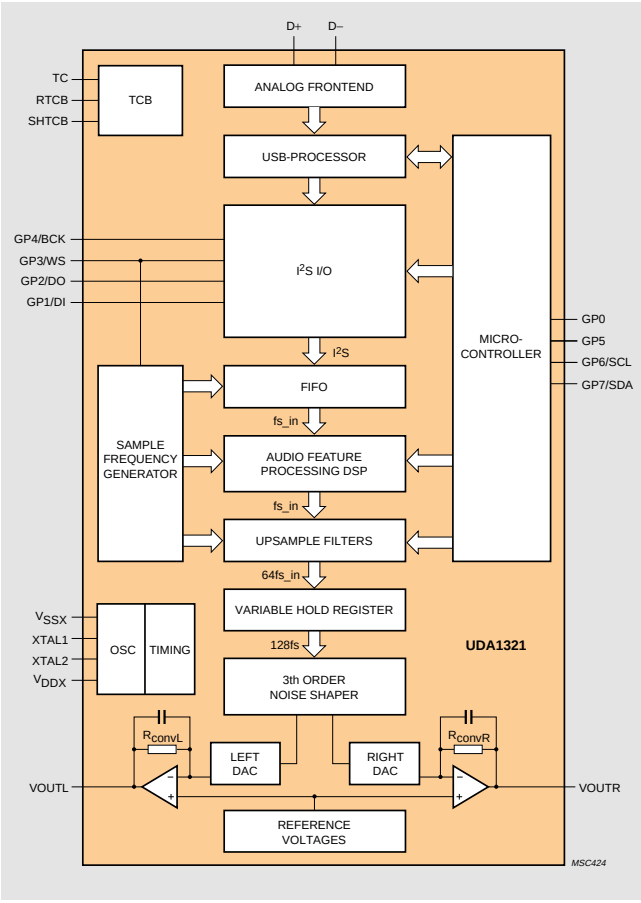
- **Complete stereo USB-DAC system with integrated filtering and line output drivers**
- **Supports all USB-compliant audio multimedia devices**
- **On-board DSP complies with USB and HID audio device class specification and provides extensive sound processing**
- **Supports 12 Mbits/s 'full speed' serial data transmission**
- **Fully automatic 'Hot Plug-and-Play' operation**
- **Supports multiple audio data I/O formats**
- **Asynchronous and isochronous support**
- **High SNR with low total harmonic distortion**
- **High linearity and wide dynamic range**
- **Digital PLL-based asynchronous Master clock**
- **Low power consumption and Power down mode under USB 'suspend' control**
- **On-chip timing reference recovery system including oscillator circuitry, using an external crystal for clock regeneration**

The UDA1321 is a stereo CMOS DAC and USB interface specifically designed for USB compliant audio devices and multimedia audio applications such as USB-equipped monitors and telephony devices, and digital audio speakers. It incorporates an analog front-end, USB processor, embedded microcontroller and an Asynchronous DAC (ADAC). The USB processor forms the interface between the USB, ADAC and microcontroller and consists of a Serial Interface Engine (SIE), a Memory Management Unit (MMU) and an Audio Sample Redistribution module.

The ADAC includes a Sample Frequency Generator which reconstructs the sample clock, digital upsampling filters, a noise shaper, a Filter Stream DAC (FSDAC) and a unique sound processing DSP to handle feature processing. Audio information can be applied to the ADAC via the USB interface, or directly as I^2S input data or LSB-justified data with word lengths of 16-, 18- or 20-bits. Two upsample filters along with a variable sample-and-hold function increase the oversampling rate from 1 f_s to 128 f_s, after which a third order noise shaper converts oversampled data to a bitstream for the FSDAC. Finally, on-board amplifiers convert the FSDAC output current to a voltage output signal for driving a line output.

Sound processing features are in line with the USB audio device class specification and include digital de-emphasis; separate digital volume control for left and right channels via USB or direct control; digital bass and treble tone control; and separate soft mute for left and right channels. Additional features can be included with the use of an external DSP IC, connected via the I^2S-bus.

QUICK REFERENCE DATA		
Supply voltage		3.3 V
I^2C-bus controlled		Yes
Digital supply current		85 mA
Audio input sample frequency range		5 – 55 kHz (continuous)
Typical THD + N at 0 dB		–85 dB
Typical THD + N at –60 dB		–30 dB
SNR		95 dB
Total power dissipation (typ.)		150 mW
Package	UDA1321	SDIL32
	UDA1321T	SO28



TDA1305T(AT)

Bitstream/CC filter DAC

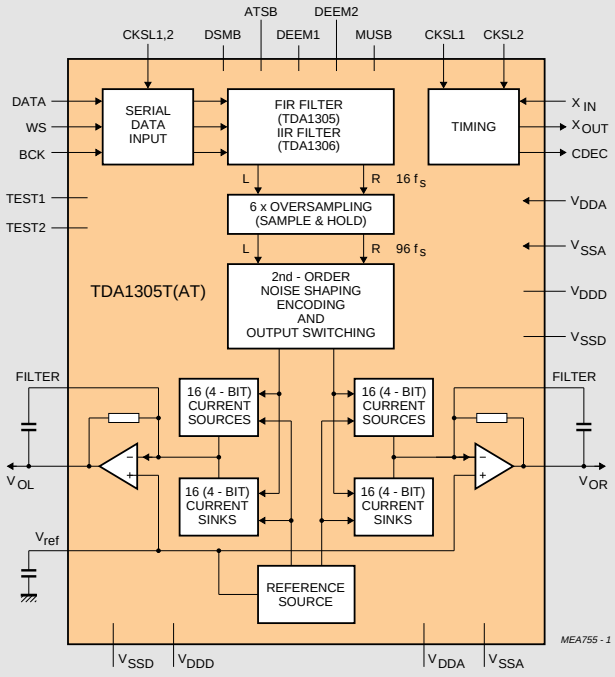
- **Cascaded 4-stage digital filter incorporating 2-stage FIR (Finite Impulse Response) filter, linear interpolation and sample and hold circuit**
- **–12 dB fixed attenuation on volume control**
- **Soft mute and noise shaping**
- **No zero crossing distortion**
- **Digital de-emphasis filter for 32, 44.1 and 48 kHz sampling rates**
- **I^2S or 'S' $1f_s$ serial input formats at 16-, 18- or 20-bits**
- **128 times oversampling at 256 × f_s; 96 times at 384 × f_s**

The TDA1305T(AT) are BCC (Bitstream/Continuous-Calibration) filter-DACs which use Philips' Bitstream conversion technique for optimum audio performance at low signal levels, and the power-saving CC technique on larger signals.

The DACs accept input in I^2S format or Japanese format with word lengths of 16, 18 and 20 bits. Four cascaded filters increase the oversampling rate to ×16. A sample-and-hold function increases the oversampling rate in normal speed mode to ×96 ($f_{sys} = 384f_s$) or ×128 ($f_{sys} = 256f_s$) or to ×48 ($f_{sys} = 256f_s$) or ×64 ($f_{sys} = 384f_s$) . A 2nd-order noise shaper converts this over-sampled data into a bitstream.

The DAC also incorporate special data encoding. This ensures an extremely high signal-to-noise ratio, superior dynamic range, and immunity to process variations and component ageing.

QUICK REFERENCE DATA	
Supply voltage	3.4 to 5.5 V
Digital de-emphasis filter for 3 sampling rates	32, 44.1, 48 kH
Typical THD at 0 dB	–90 dB
Typical THD at –60 dB	–46 dB
Typical SNR	110 dB
RMS full scale output	1.5 V
Package	SO28



TDA1388T/M

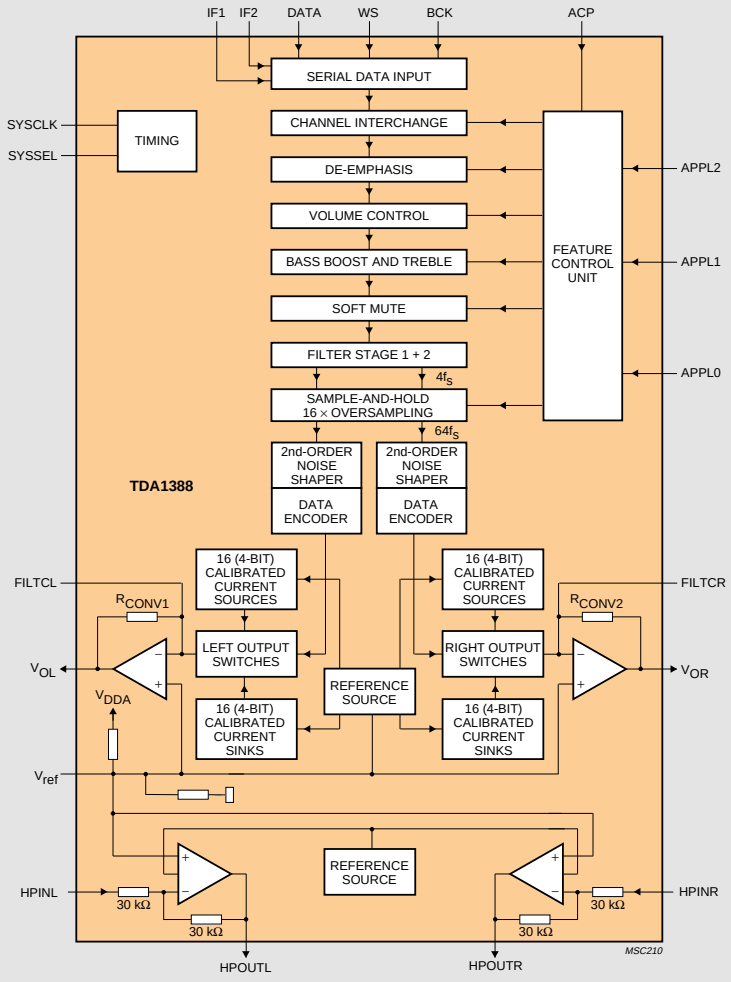
Bitstream/CC filter DAC

2

- **Single-chip audio processor**
- **On-chip filtering, DACs, postfiltering and buffering**
- **CD-ROM sound path features include separate L & R soft mute, bilingual and monaural modes, channel interchange or combinations**
- **DSP functions cover independent L & R volume control, bass and treble boost, and de-emphasis**
- **I^2S and LSB input formats**
- **Stereo line out with microprocessor-controlled volume**
- **Stereo headphone output with potentiometer volume control**
- **High linearity, wide dynamic range and low distortion**

The single-chip TDA1388 highly-integrated Bitstream/CC filter-DAC offers many sound processing functions, providing a complete sound reproduction solution in CD-ROM applications. It requires no analog postfilter and can be controlled by static pins or by microcontroller interface.

QUICK REFERENCE DATA		
Supply voltage		5 V
Supply current		22 mA
SNR		95 dBA
Dynamic range		95 dB
THD + N		–85 dB line out
		–65 dB headphone output
Total power dissipation		110 mW
Package	TDA1388T(M)	SO28 (SSOP28)



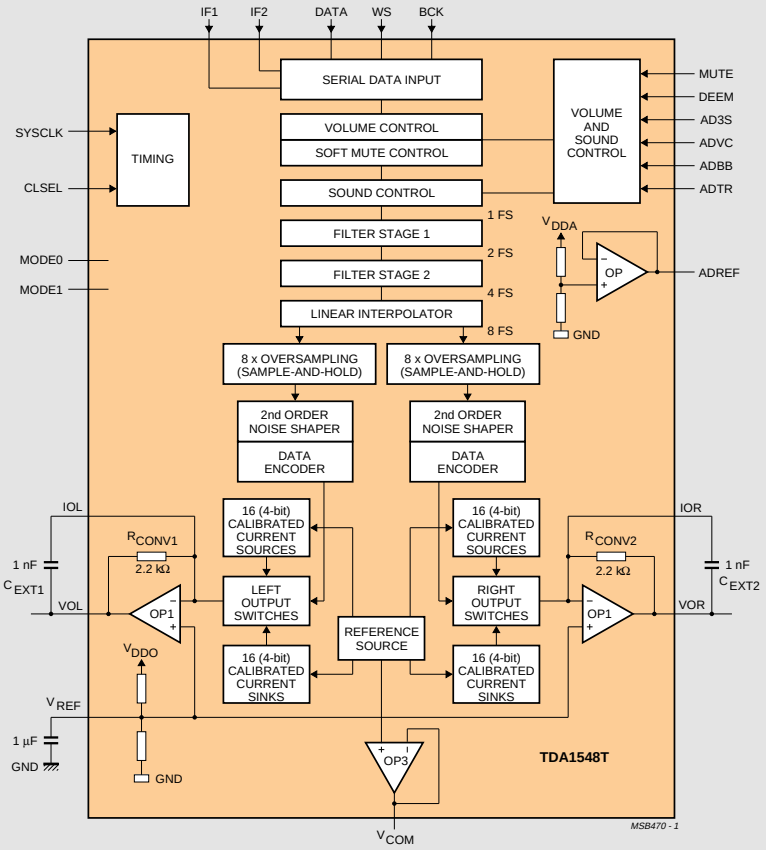
TDA1548T

Bitstream/CC filter DAC

- **Single-chip audio processor**
- **Incorporates DACs, digital de-emphasis filters, volume and tone control, and a headphone amplifier**
- **Accepts up to 20-bit serial input in I^2S or LSB-justified format**
- **Up to 128 times oversampling**
- **Cascaded 4-stage digital filter incorporates 2-stage FIR filter and linear interpolator**
- **Noise-shaping filter delivers excellent THD and noise figures**
- **Two separate dynamic ranges for the bass boost filter**
- **Soft mute**
- **No zero crossing distortion**
- **Master and slave operation**

Designed as a single-chip solution for all sound functions in CD, MD and DCC personal stereo players, the TDA1548T family of Bitstream/CC DACs also provides a complete sound channel processing solution for multimedia PC applications and dual-purpose CD-ROM drives. A selectable flat frequency response allows the headphone outputs to be used as line outputs for driving speakers and its design means no bulky DC blocking capacitors are needed in CD-ROM headphone driver applications. With its low operating voltage and small package, it is particularly suited to portable battery powered equipment, including notebook PCs.

QUICK REFERENCE DATA	
Supply voltage	3 V
Supply current	16 mA
SNR	95 dB
Selectable system clock	64, 256 and 384 f_s
THD + N at 0 dB	–85 dB
THD + N at –60 dB	–35 dB
Digital de-emphasis filter	44.1 kHz
Total power dissipation (max.)	50 mW
Package	SSOP28



TDA1549T

Bitstream continuous calibration DAC

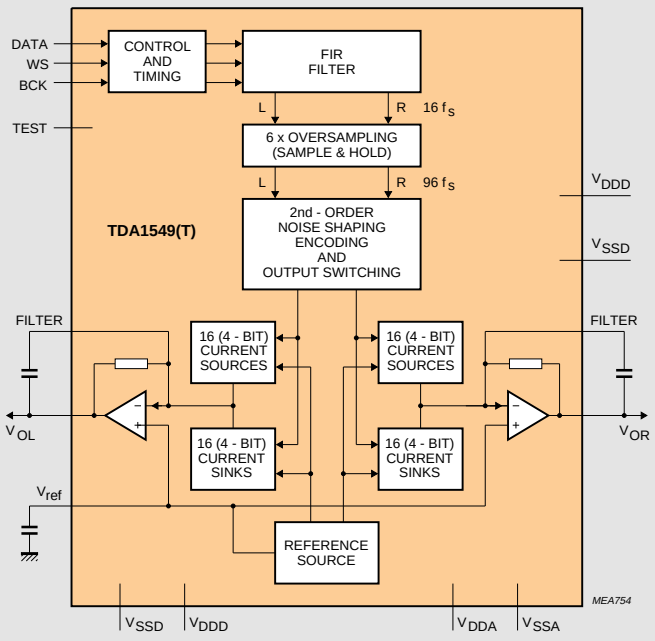
2

- **Simple application**
- **Continuous calibration DAC combined with the bitstream technique**
- **Cascaded 3-stage digital filter incorporating 7th-order half-band FIR filter stage, linear interpolator and sample and hold**
- **Noise shaper**
- **No zero crossing distortion**

The TDA1549T (BCC-DAC1) featuring a unique combination of bitstream and continuous calibration. This combination, together with a high degree of analog and digital integration, results in a digital-to-analog conversion system with true 18-bit dynamic range, high linearity and simple low-cost application.

Furthermore, the internal reference circuitry in the IC ensures that the output voltage is proportional to the supply voltage, thereby making optimum use of the supply voltage over a wide range (3.8 to 5.5 V).

QUICK REFERENCE GUIDE	
Supply voltage	3.8 to 5.5 V
Typ. THD + N at 0 dB	–90 dB
Typ. THD + N at –60 dB	–50 dB
Typical SNR	110 dB
Serial input format	"S" 4f_s, 18-bit
RMS full-scale output voltage	1.5 V
Package	SO16

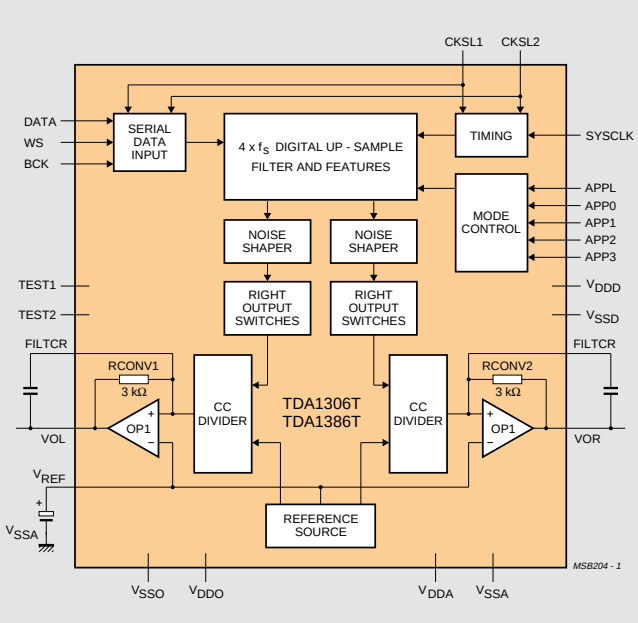


TDA1306T/TDA1386T

Continuous Calibration filter DACs

- **Simple application**
- **Noise shaping filter**
- **Cascaded 4-stage digital filter incorporating IIR filter stage**
- **–12 dB fixed attenuation on volume control**
- **Soft mute and noise shaping**
- **Variable volume control via microcontroller interface**
- **No zero crossing distortion**
- **Digital de-emphasis filter at 44.1 kHz sampling rate**
- **I^2S or 'S' 1f_s serial input formats at 16-, 18- or 20-bits**
- **4 times oversampling**
- **Selectable system clock 256 f_s or 384 f_s (TDA1306T only)**
- **TDA1305T pin compatible (TDA1306T only)**

The TDA1306T/86T dual CC-DACs are a low-cost alternative to the TDA1305T. With their up-sampling filter and noise shaping, they require only simple 1st-order analog post-filtering. Two on-board operational amplifiers convert the digital-to-analog current to an output voltage.



QUICK REFERENCE DATA	TDA1306T	TDA1386T
Supply voltage	5 V	5 V
Typical THD at 0 dB	–70 dB	–70 dB
Typical THD at –60 dB (A-weighting)	–42 dB	–42 dB
Typical SNR	110 dB	108 dB
Selectable system clock	256, 384 × f_s	256 × f_s
RMS full scale output	1.1 V	1.1 V
Package	SO24	SO24

TDA1310A(T)/TDA1387T/TDA1545A(AT)

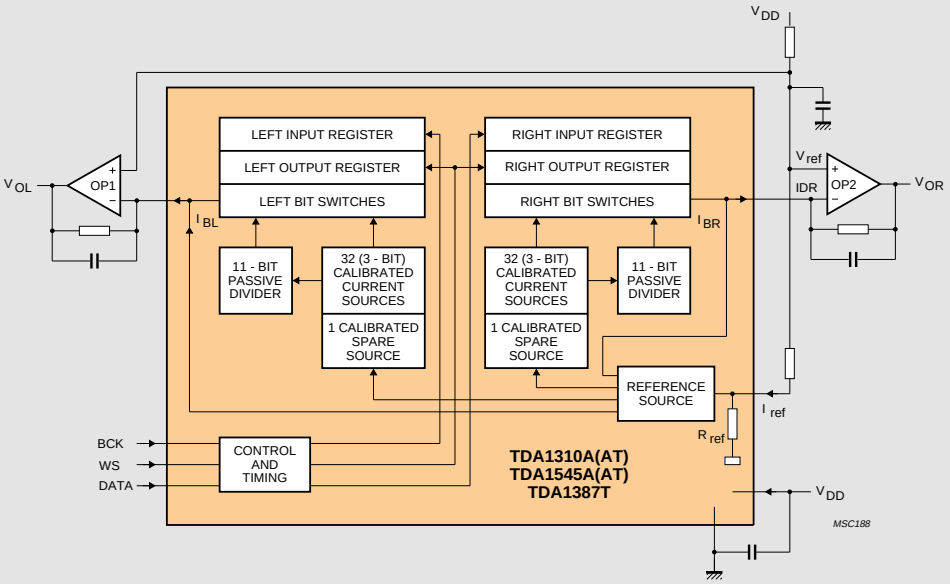
Continuous Calibration DACs with current output

- **Low power consumption**
- **Space saving SO8 package**
- **Wide operating temperature range (–40 °C to +85° C)**
- **Single 3 V to 5.5 V supply**
- **Internal bias current ensures wide dynamic range (16-bit resolution)**
- **Output current and bias current are proportional to the supply voltage**
- **Short settling time permits $2f_s$, $4f_s$ or $8f_s$ oversampling (serial input) or double-speed operation at $4f_s$ oversampling**
- **No zero-crossing distortion**

In these three DACs, 32 current sources and one spare current source are continuously calibrated. The 32 current sources define the 5 MSBs. The spare current source is included to allow continuous converter operation. The output from one of the calibrated current sources is connected to an 11-bit binary current divider containing 2048 transistors which defines the 11 LSBs.

These DACs accept 16-bit serial data input words with left and right channel words time-division multiplexed. The MSB (bit 1) must always be first. With the Word Select (WS) input HIGH, input data are placed in the left input register; with it LOW, input data are placed in the right input register. The data in the input registers are simultaneously latched to the associated output registers which control the bit switches.

QUICK REFERENCE DATA		TDA1310A/AT	TDA1387T	TDA1545A(AT)
Supply voltage		3 to 5.5 V	3 to 5.5 V	3 to 5.5 V
Supply current		3.0 mA	5.5 mA	3.0 mA
Input format		'S', up to $4 \times f_s$	I^2S up to $4 \times f_s$	'S', up to $4 \times f_s$
Full-scale output current		1.0 mA	1.0 mA	1.0 mA
Typical THD + N at 0 dB		–65 dB	–88 dB	–88 dB
Typical SNR		95 dB	98 dB	101 dB
Typical power dissipation	@5 V	15 mW	27.5 mW	15 mW
	@3 V	6.0 mW	10 mW	6.0 mW
Package		SO8, DIL8	SO8	SO8, DIL8


V DD
V OL
OP1
I BL
LEFT INPUT REGISTER
LEFT OUTPUT REGISTER
LEFT BIT SWITCHES
11 - BIT PASSIVE DIVIDER
32 (3 - BIT) CALIBRATED CURRENT SOURCES
1 CALIBRATED SPARE SOURCE
RIGHT INPUT REGISTER
RIGHT OUTPUT REGISTER
RIGHT BIT SWITCHES
32 (3 - BIT) CALIBRATED CURRENT SOURCES
1 CALIBRATED SPARE SOURCE
11 - BIT PASSIVE DIVIDER
I BR
V ref
IDR
OP2
V OR
REFERENCE SOURCE
I ref
R ref
BCK
WS
DATA
CONTROL AND TIMING
TDA1310A(AT)
TDA1545A(AT)
TDA1387T
V DD
MSC188

TDA1311A(AT)/12A(AT)/13(T)

Continuous Calibration DACs with voltage output

- **Internal bias current ensures wide dynamic range (16-bit resolution)**
- **Output current and bias current are proportional to the supply voltage**
- **Wide operating temperature range (–40 °C to +85° C)**
- **Short settling time permits $2f_s$, $4f_s$ or $8f_s$ oversampling (serial input) or double-speed operation at $4f_s$ oversampling**
- **No zero-crossing distortion**

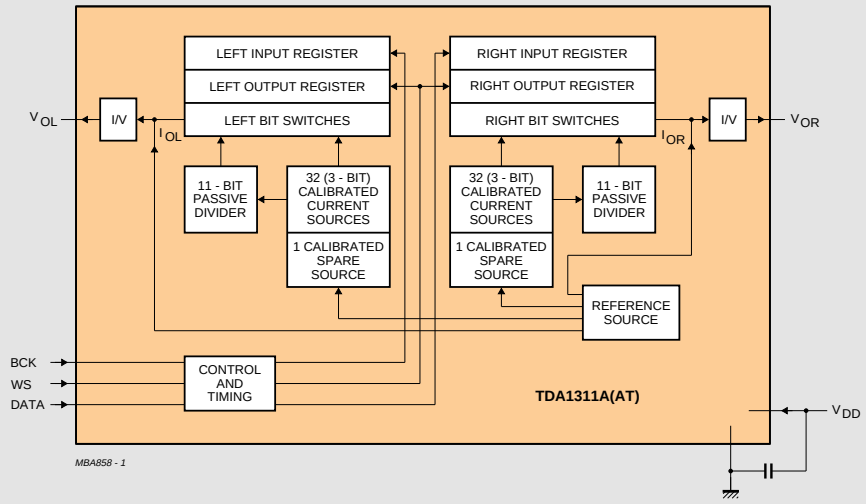
These are derivatives of the CC-DAC with current output. They include integrated I/V converters at their analog outputs. This produces a voltage output, thereby allowing the number of peripheral components to be reduced to one small decoupling capacitor.

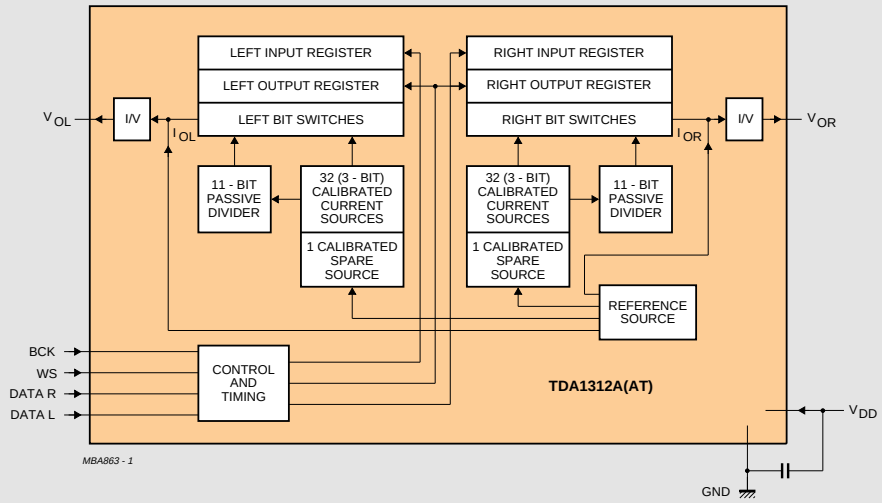
The TDA1311A(AT) version of these DACs has a $4f_s$ oversampling data input format which is compatible with most currently used non-I^2S input formats (time-division multiplexed, two's complement, TTL).

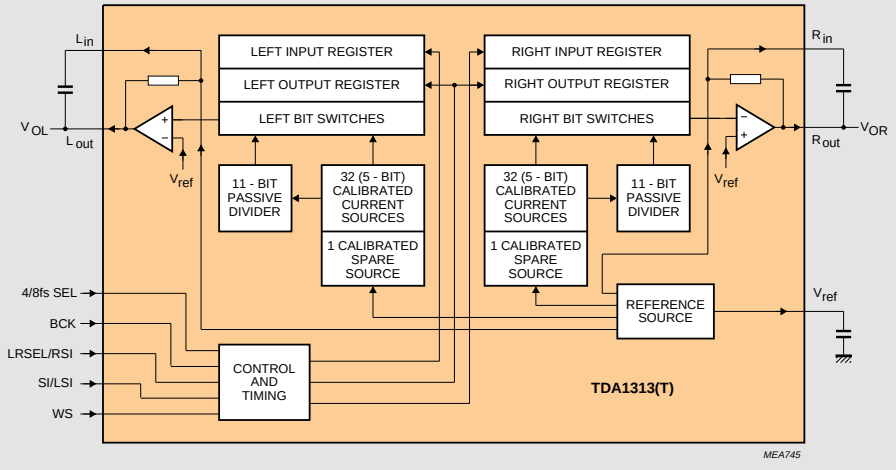
The TDA1312A(AT) can handle up to $8f_s$ oversampled data input streams which are compatible with most dual input serial data, two's complement, TTL input formats.

The final CC-DAC in this category, the TDA1313(T), is a low-noise version with selectable $4f_s/8f_s$ oversampled data input streams.

QUICK REFERENCE DATA	TDA1311A(AT)	TDA1312A(AT)	TDA1313(T)
Supply voltage	4 to 5.5 V	4 to 5.5 V	3 to 5.5 V
Supply current	3.4 mA	3.4 mA	8 mA
Input format	'S', up to $4f_s$	'S', up to $8f_s$	S", up to $4f_s$ (simultaneous) "S", up to $8f_s$ (parallel)
Full-scale output voltage	2.0 V	2.0 V	4.2 V
Typical THD + N at 0 dB	–68 dB	–68 dB	–88 dB
Typical THD + N at -60 dB	–33 dB	–33 dB	–38 dB
Typical SNR	92 dB	92 dB	98 dB
Typical power dissipation at 5 V	8 mW	8 mW	30 mW
Package	SO8, DIL8	SO8, DIL8	SO16, DIL16


LEFT INPUT REGISTER
LEFT OUTPUT REGISTER
LEFT BIT SWITCHES
RIGHT INPUT REGISTER
RIGHT OUTPUT REGISTER
RIGHT BIT SWITCHES
I/V
I/V
V OL
I OL
I OR
V OR
11 - BIT PASSIVE DIVIDER
32 (3 - BIT) CALIBRATED CURRENT SOURCES
1 CALIBRATED SPARE SOURCE
32 (3 - BIT) CALIBRATED CURRENT SOURCES
11 - BIT PASSIVE DIVIDER
1 CALIBRATED SPARE SOURCE
REFERENCE SOURCE
BCK
WS
DATA
CONTROL AND TIMING
TDA1311A(AT)
V DD
MBA858 - 1


LEFT INPUT REGISTER
LEFT OUTPUT REGISTER
LEFT BIT SWITCHES
RIGHT INPUT REGISTER
RIGHT OUTPUT REGISTER
RIGHT BIT SWITCHES
I/V
I/V
V OL
I OL
I OR
V OR
11 - BIT PASSIVE DIVIDER
32 (3 - BIT) CALIBRATED CURRENT SOURCES
1 CALIBRATED SPARE SOURCE
32 (3 - BIT) CALIBRATED CURRENT SOURCES
11 - BIT PASSIVE DIVIDER
1 CALIBRATED SPARE SOURCE
REFERENCE SOURCE
BCK
WS
DATA R
DATA L
CONTROL AND TIMING
TDA1312A(AT)
V DD
GND
MBA863 - 1


L in
R in
LEFT INPUT REGISTER
LEFT OUTPUT REGISTER
LEFT BIT SWITCHES
RIGHT INPUT REGISTER
RIGHT OUTPUT REGISTER
RIGHT BIT SWITCHES
V OL
L out
R out
V OR
V ref
V ref
11 - BIT PASSIVE DIVIDER
32 (5 - BIT) CALIBRATED CURRENT SOURCES
1 CALIBRATED SPARE SOURCE
32 (5 - BIT) CALIBRATED CURRENT SOURCES
11 - BIT PASSIVE DIVIDER
1 CALIBRATED SPARE SOURCE
REFERENCE SOURCE
V ref
4/8fs SEL
BCK
LRSEL/RSI
SI/LSI
WS
CONTROL AND TIMING
TDA1313(T)
MEA745

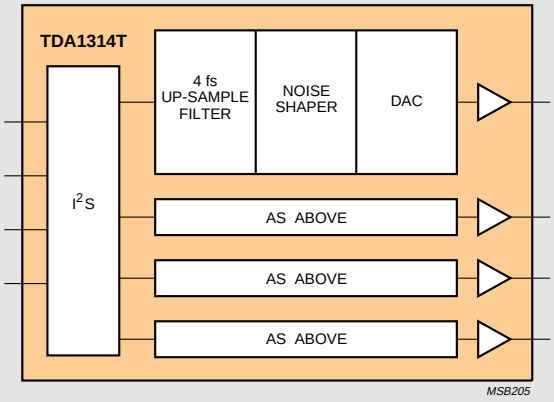
TDA1314T

Quadruple sign-magnitude filter DAC

- **Wide dynamic range (102 dB typical) allows digital (DSP) volume control**
- **Four times bit-serial oversampling filter**
- **First-order $4f_s$ noise shaper**
- **Four (front + rear stereo) very-low-noise sign-magnitude DACs for car digital audio applications**
- **Only 1st-order post filtering required**
- **Smooth power-on of the DAC output currents**
- **Automatic digital PLL divider range setting allows the master clock to be selected over a wide range**
- **Jitter on the I^2S signals does not degrade the THD**

This is a quadruple low-noise, wide dynamic range filter-DAC for use in car digital audio systems with front and rear stereo output. Each of the four channels comprises an 8th-order IIR filter with up-sampling from $1f_s$ to $4f_s$ followed by a 1st-order noise shaper and a sign-magnitude DAC. The output current is converted into a voltage by an individual operational amplifier for each of the four channels.

QUICK REFERENCE DATA	
Single supply voltage	4.75 to 5.25 V
Typ. power dissipation	85 mW
Resolution of the DACs (length of data input words)	18 bits
Typ. THD + N at full-scale at 0 dB	–70 dB
Typ. THD + N at full-scale at –60 dB	–42 dB
Typ. Digital silence (no signal, A-weighted)	–110 dBA
Serial input format	$2 \times I^2S$, $1f_s$, 18-bit with sign
Output voltage range (5 kΩ load, 3 kΩ feedback)	1 V_{RMS}
Typ. full-scale output current (R_{ref} = 20.5 kΩ)	0.5 mA
Operating temperature range	–40 to +85 °C
Package	SO28



TDA1541A/R1/S1/S2

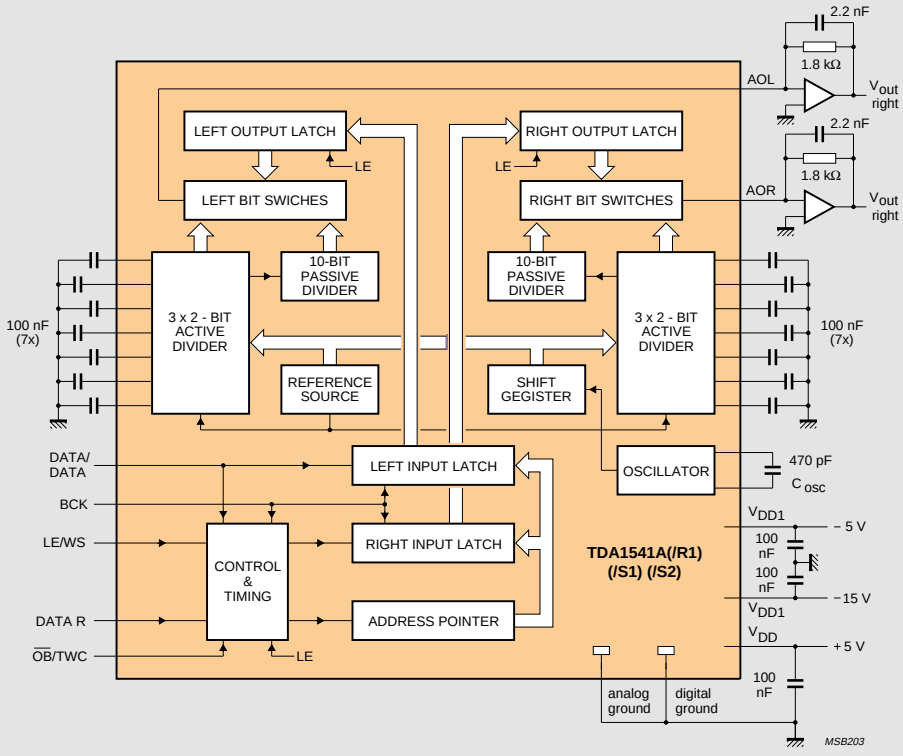
High-performance 16-bit DAC

- **Dynamic Element Matching (DEM)**
- **$4f_s$ or $8f_s$ oversampling**
- **I^2S input data format, up to $8f_s$**
- **TTL compatible inputs**
- **Marked with single crown (TDA1541A/S1 only)**
- **Marked with double crown (TDA1541A/S2 only)**

These monolithic integrated dual 16-bit digital-to-analogue converters are specifically designed for use in hi-fi digital audio equipment such as Compact Disc players, digital tape or cassette recorders.

With this range of DACs, the ten lowest bits are derived from a reference current while the six highest bits are generated by time-averaging in the Dynamic Element Matching (DEM) parts. For a full description the DEM technique.

	TDA1541A/S2	TDA1541A/S1	TDA1541A	TDA1541A/R1
Typ. THD + N at full-scale at 0 dB	–97 dB	–95 dB	–95 dB	–95 dB
Typ. THD + N at –60 dB	–47 dB	–47 dB	–42 dB	–43 dB
Channel separation	98 dB	98 dB	98 dB	98 dB
Typ. signal-to-noise ratio	112 dB	112 dB	112 dB	112 dB
Full-scale output current	4.0 mA	4.0 mA	4.0 mA	4.0 mA
Package	DIL28	DIL28	DIL28	DIL28



TDA1543(T)

Economy/low-noise 16-bit DAC

2

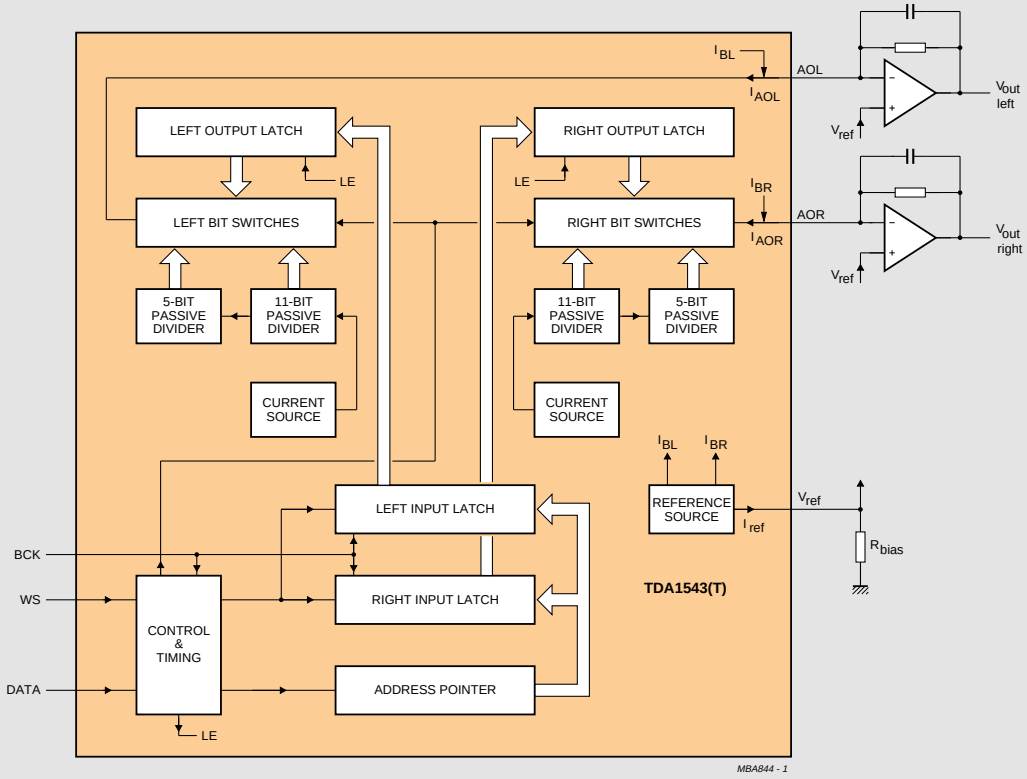
- **Low distortion**
- **16-bit dynamic range**
- **Single 5 V power supply**
- **4× oversampling possible**
- **No peripheral components required**
- **Adjustable bias current added to the output currents**

Our economy, cost-efficient 16-bit DACs are characterized by their simple application. All that's needed is a single 5 V supply and one supply decoupling capacitor.

The serial data input is shifted-in at the TTL-compatible interface. Two address pointers correctly position each data bit in the left and right input registers, and the left and right 16-bit words are simultaneously latched to the associated output registers which each drive symmetrical bit switches. Passive current dividers generate the 16 bit currents switched by the symmetrical bit switches. A low-noise current source drives left and right 11-bit passive dividers, one current from each of which is fed into an associated 5-bit passive divider to achieve a dynamic range of 16 bits. An adjustable bias current, derived from the current through the V_{REF} pin, is added to the output currents. V_{REF} can also be used as a reference for op-amps at the analog outputs.

Our low-noise 16-bit DAC is an improved version of our economy DACs with a higher signal to noise ratio and lower harmonic distortion with small signals (at -60 dB). Furthermore, it has a full-scale output current of 3 mA ±10% compared with 2.3 mA ±15% for the economy DACs.

QUICK REFERENCE DATA	
Input format	I^2S, up to $4f_s$
Typ. THD + N at full-scale at 0 dB	–75 dB
Typ. THD + N at –60 dB	–33 dB
Typical SNR	98 dB
Full-scale output current	2.30 mA
Package	DIL8, SO16



TDA1547

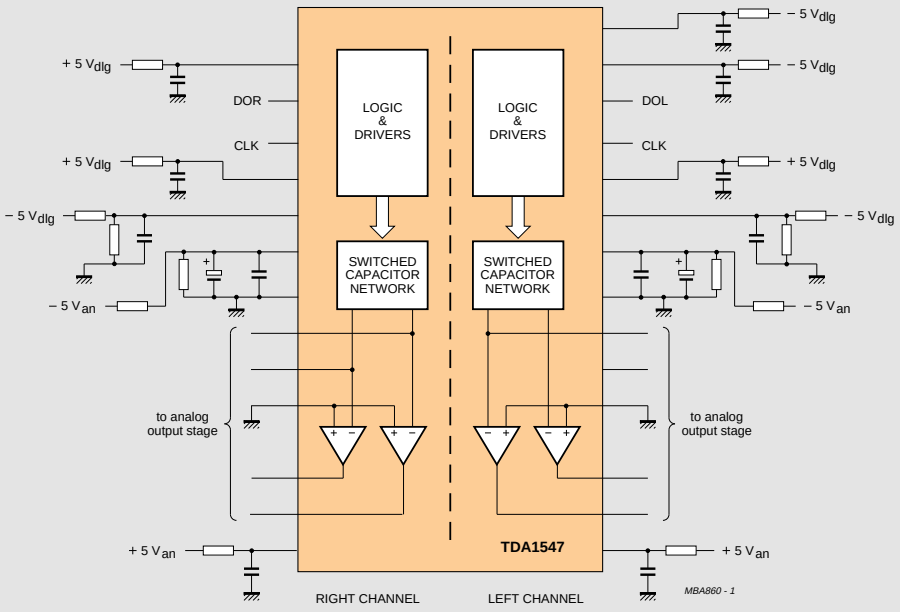
Top-performance bitstream DAC

- **Pulse density modulation**
- **Inherently monotonic**
- **No zero-crossing distortion**
- **High signal-to-noise ratio**
- **High over-sampling rate up to 192 f_s**

This top-performance bitstream DAC is a BiMOS circuit without noise shaping, digital filtering or post filtering. It is intended for use in combination with our advanced bitstream digital filter TDA1307. This results in optimum performance by reducing crosstalk between the analog and digital sections of the circuitry, extending the dynamic range, and increasing the signal-to-noise ratio. Furthermore, the BiMOS process used for the DAC allows MOS transistors to be used for the digital logic and drivers, and bipolar transistors to be used to achieve low noise analog circuitry. This optimizes speed and reduces digital noise. Other precautions taken in the DAC design to ensure maximum immunity to crosstalk are fully separated L and R channels and separate supply lines for the analog and digital sections.

It is ideally suited to high-quality audio systems such as Compact Disc and DAT players, or in digital amplifiers and digital signal processing systems.

QUICK REFERENCE DATA	
Typ. THD + N at full-scale at 0 dB	–101 dB
Typ. THD + N at full-scale at –60 dB	–51 dB
Input data format	1-bit, 192f_s
Typ. SNR	113 dB
Dynamic range	111 dB
Channel separation at 1 kHz	115 dB
RMS full-scale output voltage	1.0 V
Package	SDIL32



TDA1307

High-performance bitstream digital filter

2

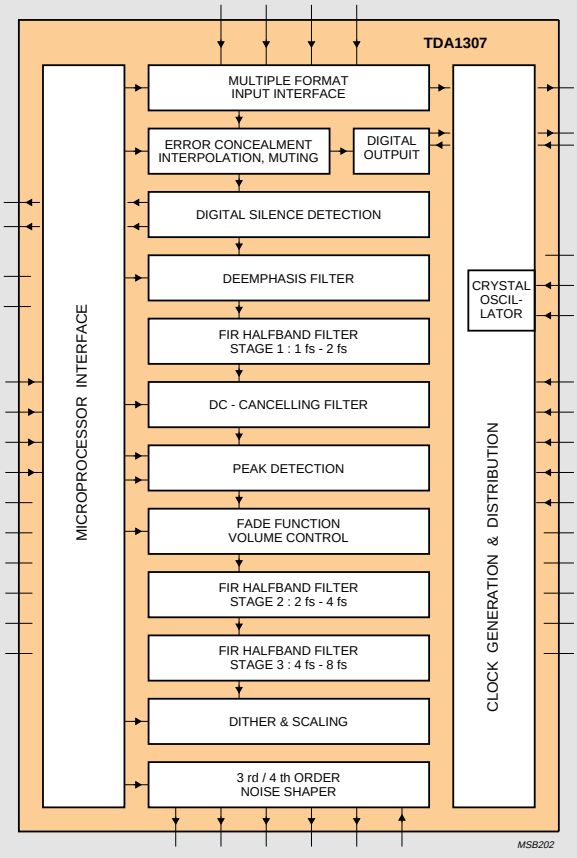
- **8-sample interpolation error concealment**
- **Digital mute: attenuation –12 dB**
- **8× oversampling Finite Impulse Response (FIR) filter; 39-bit**
- **24× up-sampling**
- **Digital audio output function (biphase-mark encoded) according to IEC958**
- **Fade function; sophisticated volume control**
- **Digital silence detection (output)**
- **DC-cancelling filter (selectable)**
- **Dedicated TDA1547 1-bit output**
- **Selectable 3rd/4th-order noise shaping**
- **Simple 3-line serial microcontroller command interface**
- **Peak detection (continuous) and readout to microprocessor**
- **Digital de-emphasis (selectable, f_s conscious); 20-bit**
- **Power-on reset**
- **Standby function**

The TDA1307 is an advanced oversampling digital filter uses is intended for use with the top-performance bitstream conversion DAC TDA1547. This two-chip approach is ideal for premium performance digital audio applications. Audio data can be applied to the input of the digital filter in I^2S, or Sony ("S") 16-, 18- or 20-bit format. A high quality bitstream is produced for application to the input of the DAC, resulting in a very high audio performance. This is largely due to the highly-accurate audio data processing structure of the filter which includes 8× oversampling, digital filtering and up to 4th-order noise shaping.

These two ICs (TDA1307 and TDA1547) achieve a high degree of versatility by providing a multitude of easily accessed functional features. Error concealment functions, audio peak data, and an advanced patented digital fade function are all accessible through a simple microprocessor command interface which also provides access to various integrated system settings and functions.

QUICK REFERENCE DATA	
Supply voltage	5 V
Supply current	75 mA
Digital audio output	32-bit words in bi-phase mark code
Input data format	I^2S, "S" 16/18/20-bit
Typ. dynamic range*	137 dB
Typ. S/N ratio*	142 dB
Package	SDIL42 (SOT270-1)

* with 4th-order noise shaper

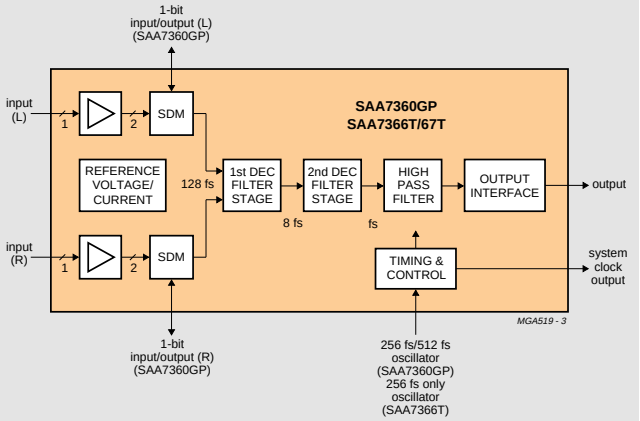


SAA7360GP/SAA7366T/SAA7367GP

Bitstream conversion ADCs

- **Stereo, single-ended inputs**
- **Input buffer for filtering and pre-scaling**
- **Fully differential ADC using 3rd-order**
- **Sigma-Delta modulation**
- **×128 oversampling, 4-stage decimation filter**
- **Switchable high-pass filter to remove DC offsets**
- **16- or 18-bit selectable output in I²S and two pseudo I²S formats (SAA7360 only)**
- **18-bit output in I²S and one pseudo I²S format (SAA7366 and SAA7367 only)**

Philips offer three bitstream conversion ADCs. They are for use in digital audio playback systems such as digital amplifiers and CD-recordable applications. Each device consists of an input buffer for pre-scaling and anti-aliasing, a 3rd-order Sigma-Delta modulator and decimation filters for anti-aliasing suppression and low in-band ripple. The choice of ADCs allows selection of high or economy performance and package type to meet the application requirements.



	SAA7360GP	SAA7366T	SAA7367GP
Supply voltage	4.5 to 5.5 V	4.5 to 5.5 V	4.5 to 5.5 V
Crystal frequency	256 or 512 × f_s	256 × f_s	256 × f_s
Sampling rate	18 to 53 kHz	18 to 53 kHz	18 to 53 kHz
Anti-aliasing suppression	>–93 dB	>–60 dB	>–60 dB
In-band ripple	<0.0002 dB	<±0.1 dB	<±0.1 dB
Min. dynamic range	93 dB	90 dB	90 dB
Typ. THD + N at –1 dB digital output	–90 dB	–88 dB	–88 dB
Analog input voltage	V_{DD}/2 ±5% V	V_{DD}/2 ±5% V	V_{DD}/2 ±5% V
Package	QFP44	SO24	SO24

UDA1325

USB CODEC

- **Complete stereo USB-COCEC system with integrated filtering and line output drivers**
- **Supports all USB-compliant audio multimedia devices**
- **Supports 12 Mbits/s “full speed” serial data transmission**
- **Fully automatic “Plug-and-play” operation**
- **Efficient power management mode**
- **On-chip master clock oscillators**
- **Soft mute**
- **External DSP option via I²S or Japanese digital I/O format**
- **On-chip digital de-emphasis**
- **Selectable clipping detection/prevention and Dynamic Bass Boost (DBB)**
- **Supports multiple audio data I/O formats**
- **High SNR with low total harmonic distortion**
- **High linearity and wide dynamic range**
- **Low power consumption**
- **Digital bass and treble tone control**
- **Partially programmable USB descriptors via I²C-bus**
- **Separate digital volume control for left and right channels**
- **Easy application and inexpensive to implement**

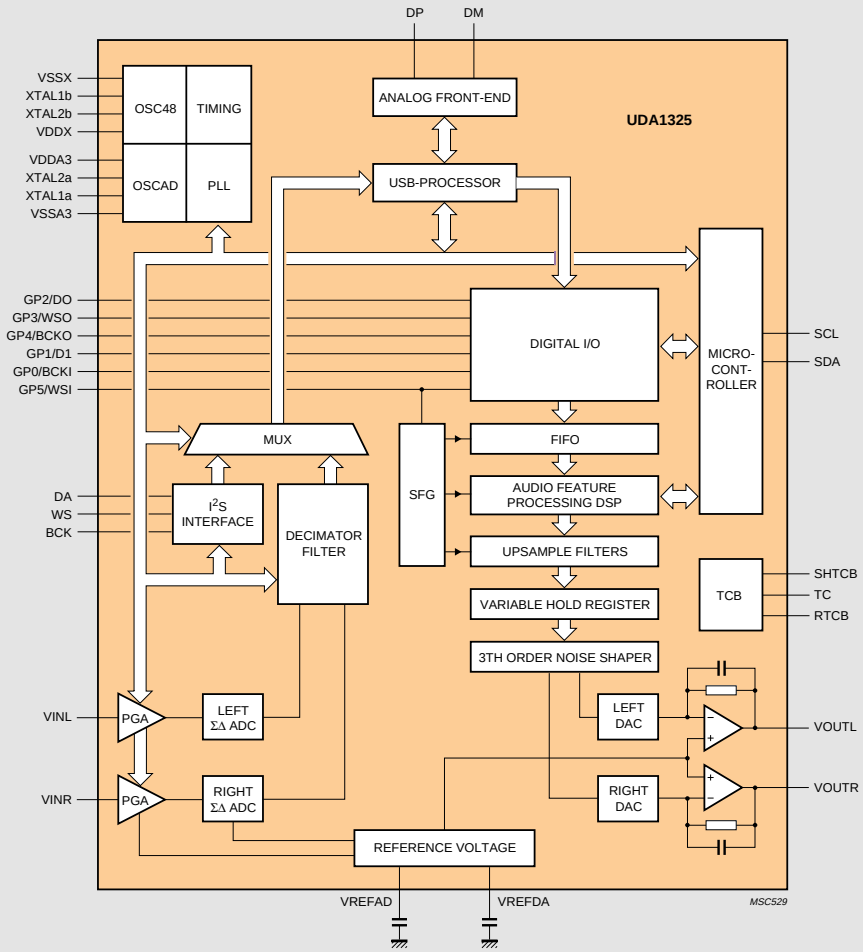
The UDA1325 is a stereo bitstreeam ADC, DAC and USB interface specifically designed for USB compliant audio devices and multimedia audio applications such as USB-equipped monitors and telephony devices, and digital audio speakers. It incorporates an analog front-end, USB processor, embedded microcontroller, an Audio-to-Digital Interface (ADIF) and an Asynchronous DAC (ADAC). The USB processor forms the interface between the USB, ADIF, ADAC and microcontroller.

The ADAC includes a Sample Frequency Generator to reconstructs the average sample frequency from the incoming audio samples, a FIFO, a unique audio-feature processing DSP to handle feature processing, digital upsampling filters, a variable hold register, a noise shaper, and a Filter Stream DAC (FSDAC) with integrated filter and line output drivers. Audio information can be applied to the ADAC via the I/O interface, or directly as I²S input data or LSB-justified data with word lengths of 16-, 18- or 20-bits.

The ADIF consists of a Programmable Gain Amplifier (PGA), an ADC and a decimator filter. The ADIF clock frequency, which is generated by either an Analog Phase Lock Loop (APPL) or oscillator, can be controlled by the microcontroller Several clock frequencies are possible for sampling the analog input signal at different sampling rates.

Sound processing features are in line with the USB audio device class specification and include digital de-emphasis; separate digital volume control for left and right channels digital bass and treble tone control; and soft mute. Additional features can be included with the use of an external DSP IC, connected via the I/O-bus.

QUICK REFERENCE DATA	
Supply voltage	5 V
I²C-bus controlled	Yes
I²S interface	Yes
Package	SDIL42, QFP44


DP
DM
VSSX
XTAL1b
XTAL2b
VDDX
VDDA3
XTAL2a
XTAL1a
VSSA3
OSC48
TIMING
OSCAD
PLL
ANALOG FRONT-END
USB-PROCESSOR
UDA1325
GP2/DO
GP3/WSO
GP4/BCKO
GP1/D1
GP0/BCKI
GP5/WSI
DIGITAL I/O
MICRO-CONT-ROLLER
SCL
SDA
MUX
FIFO
DA
WS
BCK
I2S INTERFACE
DECIMATOR FILTER
SFG
AUDIO FEATURE PROCESSING DSP
UPSAMPLE FILTERS
TCB
SHTCB
TC
RTCB
VARIABLE HOLD REGISTER
3TH ORDER NOISE SHAPER
VINL
PGA
LEFT ΣΔ ADC
LEFT DAC
VOUTL
VINR
PGA
RIGHT ΣΔ ADC
RIGHT DAC
VOUTR
REFERENCE VOLTAGE
VREFAD
VREFDA
MSC529

UDA1340M/UDA1341TS

Low-voltage, low-power stereo audio ADC/DAC with DSP features

- **Low power, low voltage (3.0 V) stereo audio CODEC**
- **ADC with integrated decimation and DC offset cancellation filtering**
- **DAC with integrated interpolation filter and noise shaper**
- **Selectable system clock frequencies (256 f_s, 384 f_s and 512 f_s)**
- **Overload detection for easy record level control**
- **Separate power control for ADC and DAC**
- **Microcontroller interface**
- **Multiple format input interface compatible with I^2S-bus, MSB-justified and LSB-justified**
- **Supports word lengths up to 20 bits (I^2S, MSB) and 16-, 18- and 20-bit (LSB)**
- **Range of digital sound processing features**
- **Stereo single-ended input configuration**
- **Stereo line output under microcontroller volume control**
- **High linearity, wide dynamic range, low distortion**
- **No analog post-filtering required**

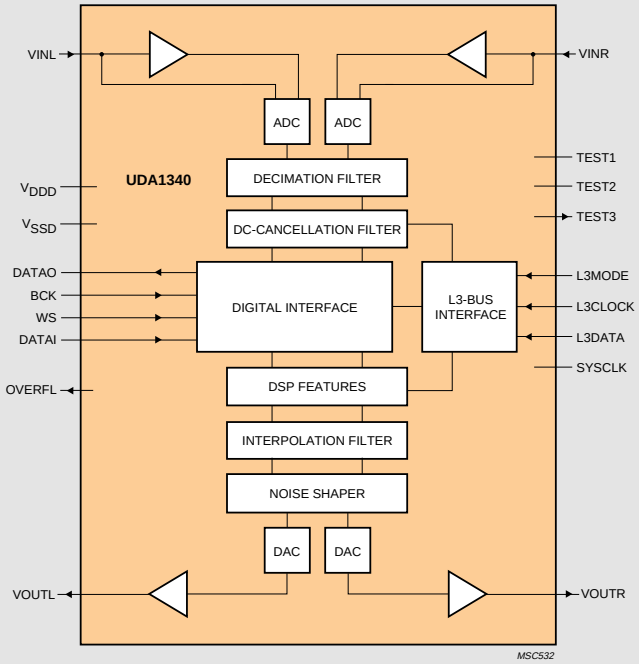
The UDA1340M/UDA1341TS are single-chip stereo bitstream A/D and D/A converter with built-in digital signal processing features. Operating from a low power supply and offering low power consumption they are ideal for portable digital audio applications incorporating playback and recording functions.

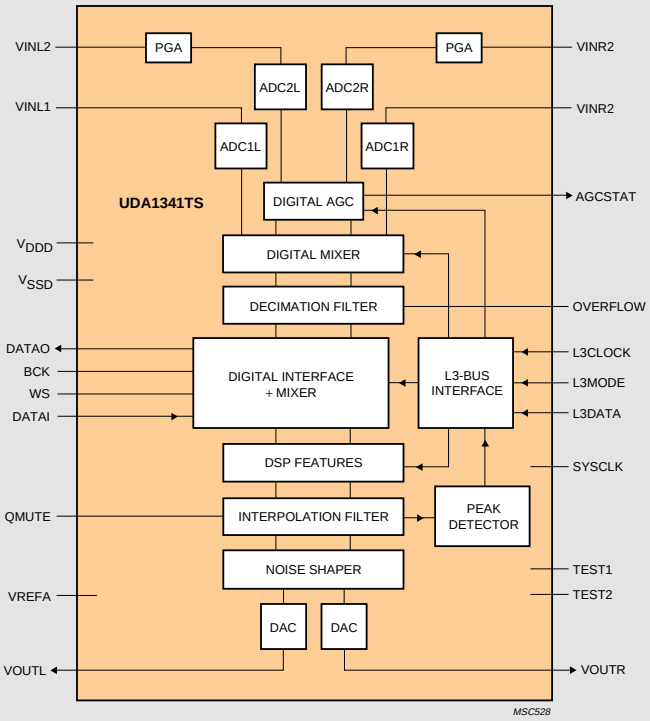
DSP features for audio playback, all of which can be controlled via the microcontroller interface, include digital volume control, bass and treble boost, dB-linear volume and tone control, digital de-emphasis (32 kHz, 44.1 kHz and 48 kHz f_s) and soft mute.

The UDA1341TS is simmilar to the UDA1340M but with added fesatures, such as mixing of two analog signals, as well as mixing signals from the ADC with the digital input signal and digital Automatic Gain Gontrol (AGC).

Both ICs support the I^2C-bus and MSB-justified data format with word leangths of up to 20-bits, and the LSB-justified serial data format with word leangths of 16, 18 and 20-bits.

QUICK REFERENCE DATA		UDA1340M	UDA1341TS
Supply voltage		2.7 to 3.6 V	2.7 to 3.6 V
ADC	Analog supply current	4.5 mA	12 mA
	Digital supply current	3 mA	t.b.d.
	Typical THD + N at 0 dB	–85 dB	–90 dB
	SNR	95 dB	100 dB
DAC	Analog supply current	3.5 mA	6.0 mA
	Digital supply current	3 mA	t.b.d.
	Typical THD + N at 0 dB	–95 dB	–95 dB
	SNR	100 dB	102 dB
Total power dissipation (typ.)	ADC	27 mW	45 mW
	DAC	33 mW	33 mW
Package		SSOP28	SSOP28


VINL
VINR
ADC
ADC
UDA1340
TEST1
TEST2
TEST3
VDDD
VSSD
DECIMATION FILTER
DC-CANCELLATION FILTER
DATAO
BCK
WS
DATAI
DIGITAL INTERFACE
L3-BUS INTERFACE
L3MODE
L3CLOCK
L3DATA
SYSCLK
OVERFL
DSP FEATURES
INTERPOLATION FILTER
NOISE SHAPER
DAC
DAC
VOUTL
VOUTR
MSC532


VINL2
PGA
PGA
VINR2
ADC2L
ADC2R
VINL1
VINR2
ADC1L
ADC1R
UDA1341TS
DIGITAL AGC
AGCSTAT
VDDD
VSSD
DIGITAL MIXER
DECIMATION FILTER
OVERFLOW
DATAO
BCK
WS
DATAI
DIGITAL INTERFACE + MIXER
L3-BUS INTERFACE
L3CLOCK
L3MODE
L3DATA
DSP FEATURES
SYSCLK
QMUTE
INTERPOLATION FILTER
PEAK DETECTOR
NOISE SHAPER
TEST1
TEST2
VREFA
DAC
DAC
VOUTL
VOUTR
MSC528

TDA1309H/UDA1309H

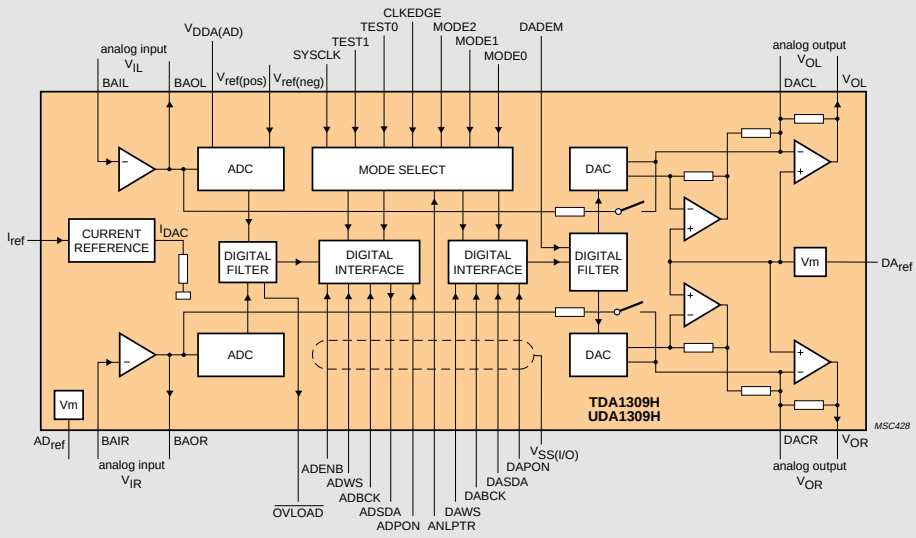
Low-power, (low-voltage) stereo ADC/DAC

2

- **Low power stereo CODEC**
- **2.7 V low-voltage version (TDA1309H)**
- **Bitstream ADC and bitstream/CC DAC**
- **Separate power down modes for ADC and DAC**
- **Integrated high-pass filter to cancel DC offset (ADC)**
- **Analog loop through function**
- **256 f_s system clock frequency for ADC and DAC**
- **192 f_s, 256 f_s and 384 f_s DAC clock frequencies**
- **Digital de-emphasis (DAC)**
- **Multiple digital I/O formats**
- **Overload detector enabling automatic recording level adjustment (ADC)**
- **DAC requires only one capacitor for analog post-filtering**

The TDA1309H/UDA1309H combines a bitstream ADC sampling stereo left and right channels simultaneously, with a bitstream/CC DAC to provide a low power stereo CODEC for digital equipment with recording and playback functions. Operating down to 2.7 V, the TDA1309H low-voltage version is particularly suitable for portable applications.

Separate power down modes on both ADC and DAC allow power reduction when either section is not in use and the loop through function bypasses the ADC/DAC and filtering for analog recording/playback, further reducing consumption. 16- and 18-bit I^2S-bus and LSB fixed formats are supported.



QUICK REFERENCE DATA		TDA1309H	UDA1309H
Supply voltage		3 V	5 V
ADC	Analog supply current	8 mA	9 mA
	Digital supply current	0.2 mA	0.2 mA
	Typical THD + N at 0 dB	–85 dB	–85 dB
	SNR	95 dB	95 dB
DAC	Analog supply current	24 mA	28 mA
	Digital supply current	20 mA	24 mA
	Typical THD + N at 0 dB	–90 dB	–90 dB
	SNR	104 dB	104 dB
Total power dissipation (typ.)	ADC	72 mW	140 mW
	DAC	60 mW	120 mW
Package		QFP44	QFP44

DEDICATED SIGNAL PROCESSORS

MPEG devices

The perceptual audio encoding/decoding scheme defined within the ISO/IEC MPEG-1 (Motion Picture Expert Group) Audio Standard (11172-3) results in considerable reduction of the quantity of data required for digital audio, yet maintains a high level of perceived sound quality. The coding is based on a psy-cho-acoustic model of the human auditory system and exploits the fact that weak spectral components are inaudible if they are in the proximity (in both time and frequency) of loud compo-nents. This phenomenon is called masking.

Layers I and II of ISO/MPEG-1 reduce the data by splitting the broadband audio source signal into 32 sub-bands of equal width. The masking threshold (the amount of imperceptible audio energy as a function of frequency) is determined for the given signal by using the psycho-acoustic model. The sub-band samples are then re-quantized to an accuracy that ensures that the spectral distribution of the re-quantization noise does not exceed the masking threshold. This reduction of representation accuracy provides the reduction of the audio data. The re-quan-tized sub-band samples are multiplexed with side information concerning the actual re-quantization to form the MPEG audio bitstream.

During decoding, the MPEG audio bitstream is de-multiplexed and the side information is used to reconstruct the sub-band sig-nals which are combined to form a broadband audio output sig-nal.

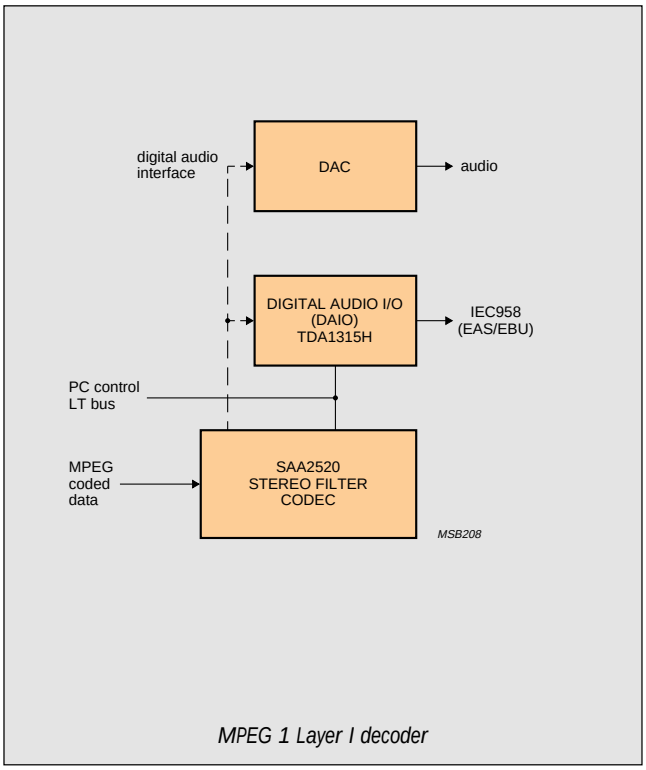
Examples of a stereo filter/CODEC for an MPEG-1 Layer I decoder and a masking threshold processor for an MPEG-1 Layer I encoder using our MPEG ICs are given below. More detailed information on these and other MPEC devices, as well as our range of dedicated signal processing ICs is given on the following pages.

Stereo filter/CODEC for an MPEG-1 Layer I decoder

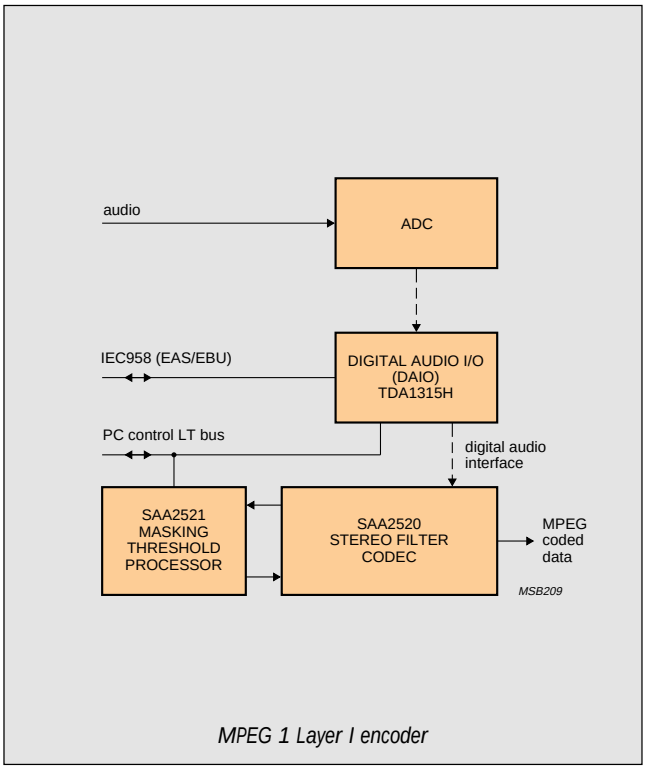
An MPEG-1 Layer I decoder can be implemented by using the stereo filter/CODEC SAA2520GP together with a digital audio input/output (DAIO) circuit TDA1315H and a stereo DAC as shown in the top figure.

Masking threshold processor for an MPEG-1 Layer I encoder

An MPEG-1 Layer I encoder can be implemented by using the masking threshold processor SAA2521 with a stereo filter/CODEC SAA2520GP, a digital audio input/output (DAIO) circuit TDA1315H, and a stereo ADC as shown in the bottom figure.



MPEG 1 Layer I decoder



MPEG 1 Layer I encoder

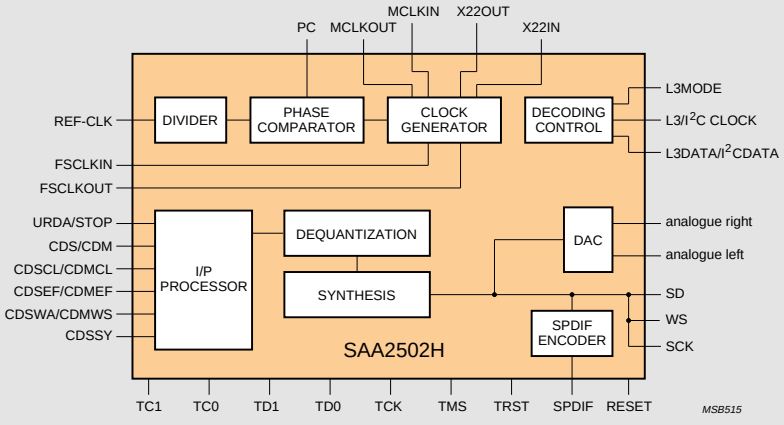
SAA2502

Audio MPEG decoder

- **Supports all MPEG-1 layer-I and layer-II audio modes**
- **Supports all MPEG-1 bit rates and sample frequencies with fully automatic switching**
- **L3 microcontroller interface**
- **Burst mode data input**
- **Programmable variable bit output precision (16-, 18-, 20- or 22-bit)**
- **Integrated audio post processing for control of signal level and inter-channel crosstalk**
- **De-multiplexing of ancillary data in input bitstream**
- **Sample clock switching and on-chip clock generation**
- **Automatic digital de-emphasis of decoded audio signal**
- **Error concealment**
- **Low power consumption**
- **MPEG-2 compatible stereo output**
- **Supports low sample frequencies (16, 22.05 and 24 kHz) with CRC correction of scale factors**
- **Handles byte- and non-byte-aligned input data**
- **IEC958 digital output**
- **Programmable automatic internal dynamic range compression algorithm**
- **Output formats include I^2S, SPDIF and 256 (or more) oversampled analog stereo**

The SAA2502 is a second generation device developed for a wide range of broadcast digital audio applications including digital radio. It is a high feature, general purpose, MPEG-2 decoder supporting both layer-I and layer-II of the MPEG-1 standard as well as meeting all requirements for a stereo MPEG-2 decoder.

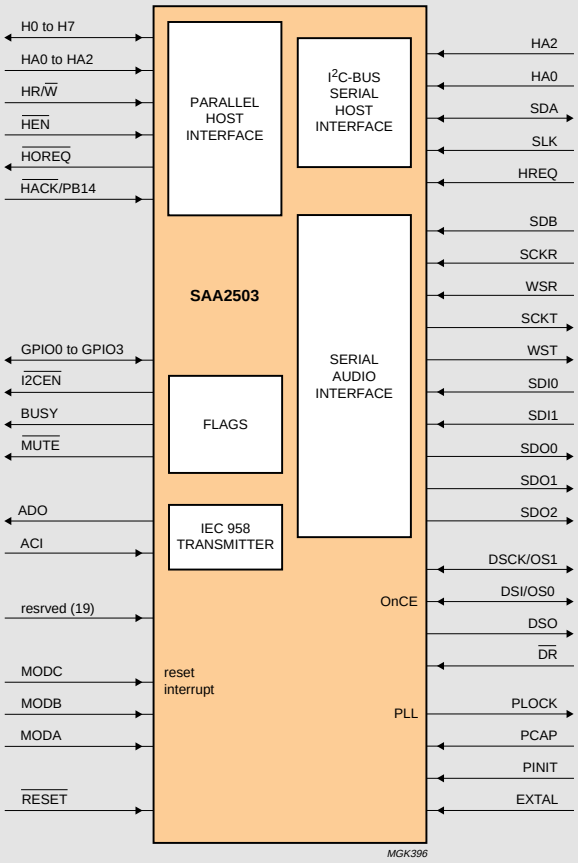
QUICK REFERENCE DATA	
Supply voltage	5 V
I^2S interface	Yes
I^2C-bus controlled	Yes
Package	QFP44



SAA2503

MPEG2 audio decoder

- **Single-chip MPEG2 multichannel audio decoder**
- **Decodes MPEG high quality audio:**
- **MPEG1 layer 2 (44.1 kHz)**
- **MPEG2 multichannel layer 2 (48 kHz)**
- **Supports pause frames**
- **Outputs 2 channels**
  - **quasi surround down-mixing for Left and Right Dolby surround channel (Lt and Rt)**
  - **stereo down-mixing for stereo reproduction**
  - **stereo signal selection**
  - **single channel down-mixing**
- **Karaoke modes**
- **Linear PCM modes:**
  - **down-sampling from 96 to 48 kHz**
  - **pass 48 kHz signals**
- **IEC 958 output interface (IEC 1937 formatted)**
- **IEC 958 output simultaneously available while decoding MPEG2**
- **Output flags for direct control**
- **Stand-alone operation possible (self-booting)**
- **No external DRAM or SRAM required**
- **On-chip PLL for internal clock generation**
- **3.5 or 27 MHz master clock**



The SAA2503 is the latest addition to our range of audio MPEG decoders. Although primarily developed for DVD players, its advanced specifications also make it ideally suited to any MPEG2 audio bitstreams application such as set top boxes, multimedia PCs and digital television.

With its MPEG2 multichannel audio decoding plus down-mixing, MPEG1 layer 2 decoding , Linear PCM (LPCM) processing , IEC 958 transmitter and serial audio interfaces, the SAA2503 brings together all the necessary audio functions of a DVD player on a single chip.

QUICK REFERENCE DATA	
Supply voltage	5 V
I²C-bus control	Yes
I²S interface	Yes
Package	LQFP100

SAA2505

DUET

Decoding functions:

- **MPEG II Layer 2 decoding for 7.1, 5.1, 2 channels**
- **MPEG 48 kHz sample rate, bitrate upto 960 kbit/s, including variable bitrate**
- **Dolby AC-3 decoding for 5.1 and 2 channels**
- **AC-3 48 kHz sample rate, bitrate upto 448 kbit/s**
- **MPEG II/AC-3 2 channels with Dolby Pro-Logic decoding**
- **MPEG II/AC-3 Multi-channel decoding with Dolby Pro-Logic encoding**
- **DVD compatible Karaoke decoding**
- **DVD Linear PCM modes converted to 48 kHz sample rate and 20 bit**

Output functions and sound effects:

- **Output configuration for 7, 5, 4, 3, 2, 1 channels with or without LFE**
- **Bass redirection for small satellite loudspeakers plus subwoofer**
- **Adjustable time delay upto 15 ms for MC-Surround or upto 30 ms for Pro-Logic**
- **Adjustable dynamic range compression for MPEG and AC-3**
- **Generation of pseudo surround signals from 2 channel input**
- **Virtual Surround effect from 2 loudspeakers**
- **Pink noise generator for loudspeaker adjustment**
- **S/PDIF (IEC-958) output of PCM or packetized bitstream**

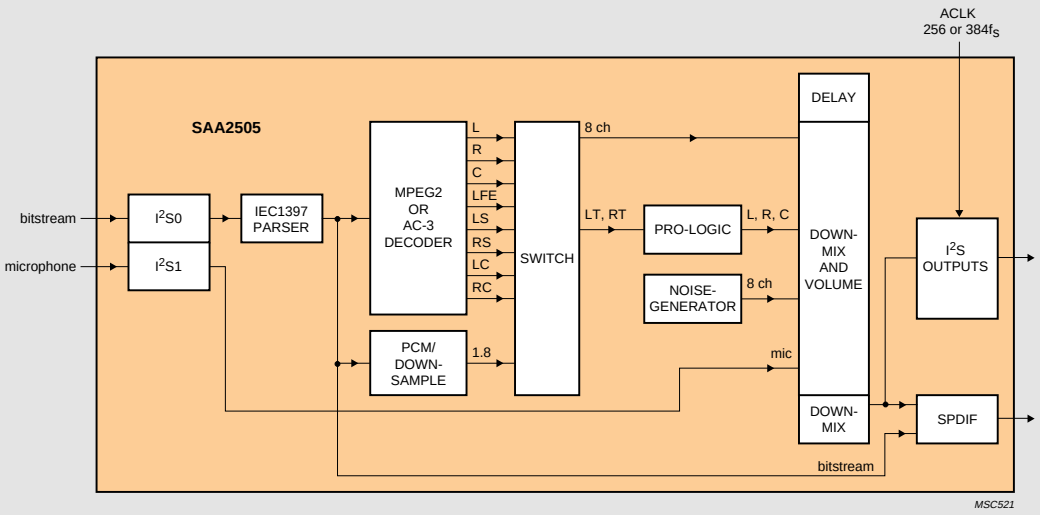
Hardware Features:

- **2 serial inputs, 4 serial outputs**
- **400 kHz I²C control interface**

The SAA2505 decodes MPEG2 7.1 channels, AC3 5.1 channels, and 8 channel Linear PCM audio signals, and its output can be configured for 7, 5, 4, 3, 2, or 1 channels with or without LFE (subwoofer). The bass signal can be redirected to the subwoofer, so that smaller satellite loudspeakers can be used.

The chip can generate pseudo surround signals from a two channel input resulting in 3D virtual surround effects from two loudspeakers. Karaoke from AC3 and MPEG has also been implemented, giving the possibility for a second serial input to be mixed into the main signal. The IC contains all the ROM, RAM and DSP cores needed for single-chip operation.

QUICK REFERENCE DATA	
Supply voltage	3 V
Input and output voltages	5 V (TTL compatable)
Package	QFP64



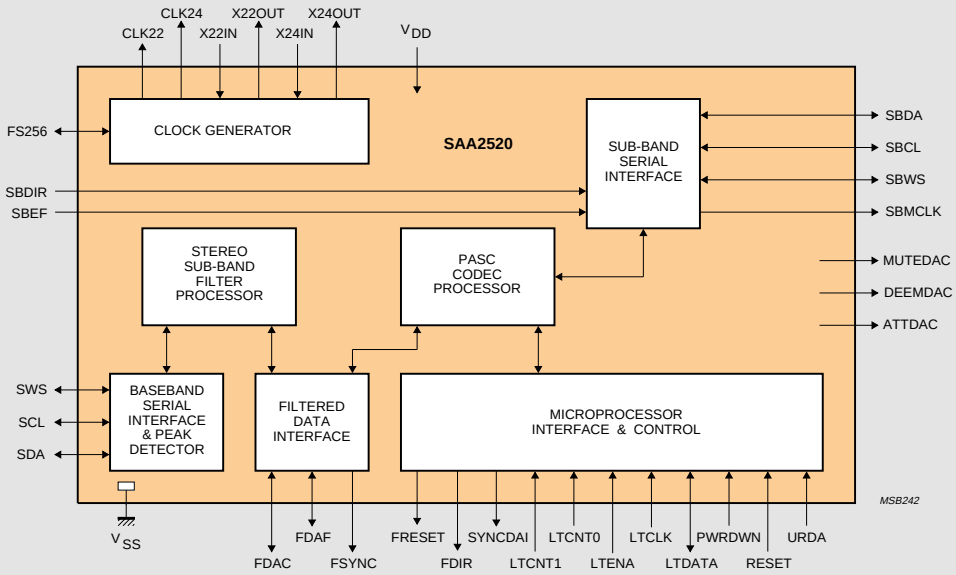
SAA2520GP

Stereo filter and CODEC for MPEG layer 1 audio applications

- **Stereo filter/CODEC**
- **Layer I compatible**
- **Microcontroller interface**
- **Low power consumption**
- **I²S interface**
- **Clock generator**
- **Required for Layer I encoding**
- **Options for Layer I decoding**
- **Microcontrolled and stand-alone modes**
- **Stereo**
- **Sample clock switching**
- **Variable bit precision**

The SAA2520 performs the sub-band filtering and audio frame CODEC functions to provide efficient audio compression/ decompression for MPEG (11172-3) Layer1 applications. It is capable of functioning as a stand-alone decoder but requires the addition of the adaptive masking threshold processor SAA2521 to function as a highly efficient encoder.

QUICK REFERENCE DATA	
Supply voltage	3.8 to 5 V
Operating temperature range	–40 to 85 °C
Package	QFP44



SAA2521GP

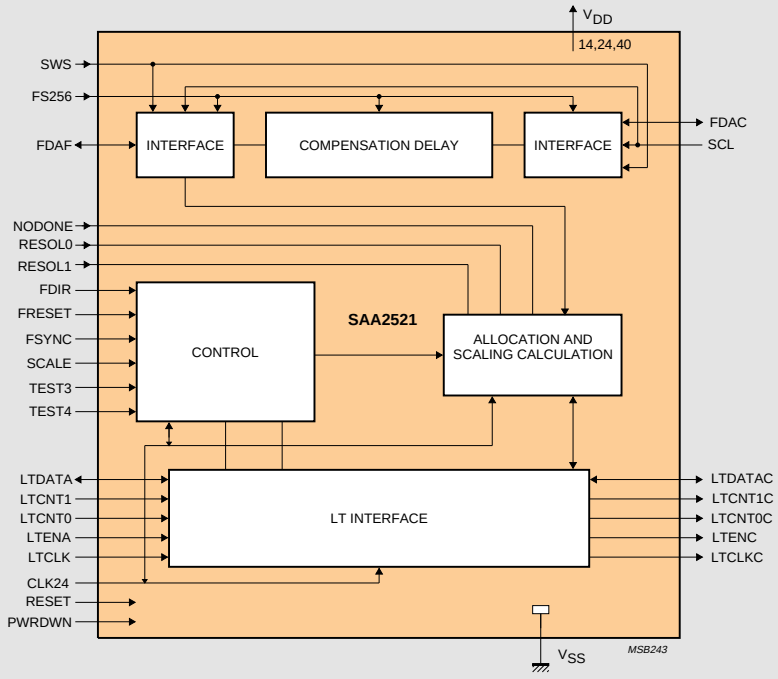
MPEG masking threshold processor

- **Masking threshold processor**
- **Layer I compatible**
- **Microcontroller interface**
- **Low power consumption**
- **I²S interface**
- **Required for Layer I encoding**
- **Stereo**
- **Sample clock switching**
- **Variable bit precision**

The SAA2521 performs the adaptive allocation and scaling function for calculating the masking thresholds and sub-band sample accuracy in MPEG layer 1 applications.

The SAA2521 is intended for use in conjunction with the stereo filter CODEC SAA2520.

QUICK REFERENCE DATA	
Supply voltage	3.8 to 5 V
Operating temperature range	–40 to 85 °C
Package	QFP44



SAA2003

Stereo filter and CODEC

- **Single-chip stereo filter and codec**
- **Wide operating voltage range**
- **Low-power consumption**
- **Sleep mode for low power and low EMI**
- **Transparent serial audio data mode in sleep**
- **IEC 958 digital output**
- **Peak level detector for start of track detection or VU meter**
- **Versatile fade processor; slow/fast fade, mute, 12 dB attenuation**
- **Serial audio interface for I^2S or EIAJ formats**
- **Error concealment**
- **Three-wire L3 bus microcontroller interface**

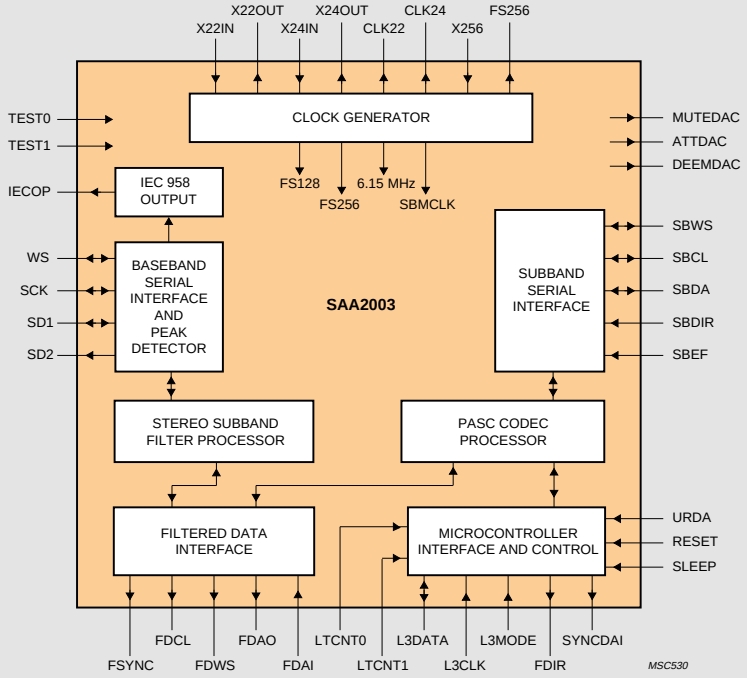
Three sample rates: 32, 44.1 and 48 kHz

Internal or external clock source

Three programmable outputs

The SAA2003 performs the sub-band filtering and audio frame CODEC functions in a Precision Adaptive Sub-band Coding (PASC) system. Although it can be used as a stand-alone decoder for playback-only applications, it requires the Adaptive Allocation and Scale Factor processor SAA2013 to perform PASC encoding in a DCC record system.

QUICK REFERENCE DATA	
Supply voltage	2.7 to 5.5 V
Supply current	
@ 3 V	32.5 mA
@ 5 V	68.8 mA
in sleep mode	400 µA
Package	QFP44



SAA2013

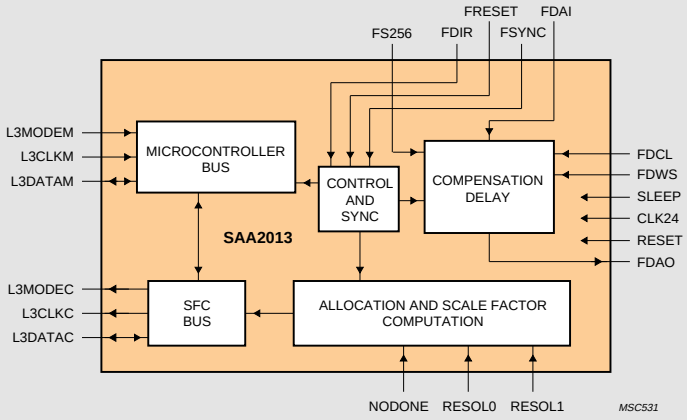
Adaptive allocation and scaling for PASC coding in DCC systems

- **Wide operating voltage range**
- **Low power consumption: 13 mW @ 3.0 V**
- **Low power decode mode: 1 mW @ 5.0V**
- **Sleep mode for low power and low EMI**
- **Sophisticated allocation algorithm**
- **Optimum sound quality**
- **Three-wire L3 bus microcontroller interface**
- **Stereo or 2-channel mono recording**

The SAA2013 performs the adaptive allocation and scaling function in a Precision Adaptive Sub-band Coding (PASC) system. It is only used during recording, and so is not required in playback-only applications.

To complete the PASC processor, the SAA2003 stereo filter and CODEC is required.

QUICK REFERENCE DATA	
Supply voltage	2.7 to 5.5 V
Supply current	
@ 3 V	5 mA
@ 5 V	10 mA
in sleep mode	400 µA
Package	QFP44



SAA7740H

Digital audio processing IC (DAPIC)

Hardware features

- **Two digital audio inputs in the I^2S format (four audio channels)**
- **Two digital audio outputs in the I^2S format (four audio channels)**
- **Independent input and output interfaces**
- **Slave input and output interfaces**
- **Slave processing**
- **I^2C microcontroller interface**
- **DC filtering at the inputs**
- **One programmable 2nd-order digital filter unit**
- **Two MAC units (24×16 bits/MAC)**
- **DRAM interface and address computation unit for external delay lines**
- **On-chip coefficient and external delay-line address storage**
- **Hard-controlled soft mute via the MUTE pin**
- **Hard-controlled soft de-mute via the RESET pin**

Software features

- **5-band parametric equalizer with selectable centre freq., slope and boost/cut gain settings of ±12 dB**
- **Stereo width control from mono to stereo to spatial stereo**
- **Stereo listening environment acoustic effects (e.g. concert hall) with 8 coefficients and 8 delayed taps per channel**
- **External delay-line processing for delays of up to 1 s**
- **Reverberation with selectable reverberation time (up to 5 s) and energy**
- **Three different surround sound programs to obtain a spatial effect with four loudspeakers**
- **Passive Dolby surround sound processing, with addition of an external dynamic noise reduction IC**
- **Karaoke processing**
- **Dual 16th-order correction filtering**
- **Quad 8th-order correction filtering**
- **Digital volume and balance control**
- **Soft-controlled soft mute/de-mute via the micro-controller interface**
- **Input switching matrix**
- **Output front and rear switching matrix**

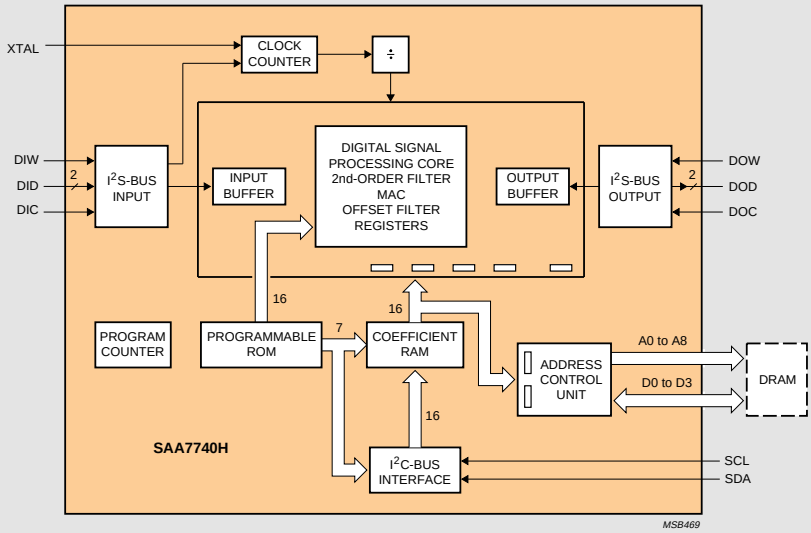
This is a very flexible function-specific 4-channel digital signal processor (DSP) for audio signals. In the general DAPIC mode, it can provide listening environment enhancements such as equalization, concert hall-effects, reverberation, surround sound/karaoke processing, and digital volume/balance control.

In the dual/quad filter modes, the IC can also be reconfigured as a dual or quad digital filter with programmable frequency characteristics. A stereo expansion mode provides stereo digital filtering, 5-band graphic equalization and complex stereo expansion for headphone out-of-head and incredible stereo applications.

Function parameters, correction coefficients and a number of configurations can be downloaded to the IC via an I^2C-bus interface.

QUICK REFERENCE DATA	
Supply voltage range	4.5 to 5.5 V
Total supply current (f_c = 16.9344 Mhz)	145 mA
Total power dissipation (f_c = 16.9344 Mhz)	700 mW
Typical crystal frequency	16.9344 MHz
Operating temperature range	–40 to +85 °C
Package	QFP64

SAA7740H



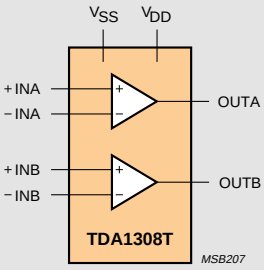
3

TDA1308T

Class AB stereo headphone driver

- **Large output voltage swing**
- **No switch ON/OFF clicks**
- **Excellent power supply ripple rejection**
- **Short circuit resistance**
- **Low power consumption**
- **High performance; high S/N ratio, high slew rate, low distortion**

The TDA1308T is a high performance integrated class AB headphone driver providing a high SNR and slew rate, combined with low distortion. Fabricated with a 1 µm CMOS process and available in either a DIP8 or surface-mount SO8 package gives this IC the low power consumption and small size which is vital for battery-powered portable digital audio applications.



QUICK REFERENCE DATA		
Supply voltage	Single	5 V (3 to 7 V)
	Dual	2.5 V (± 1.5 to ± 3.5 V)
Supply current		3 mA
Typical power dissipation		15 mW
SNR		110 dB
Typical THD + N at 0 dB		–70 (0.03) dB%
Power supply ripple rejection		90 dB
Channel separation		70 dB
Maximum output power		60 mW
Operating temperature		–40 to +85 °C
Package	Single	DIP8
	Dual	SO8

SAA7710T

Dolby surround sound circuit

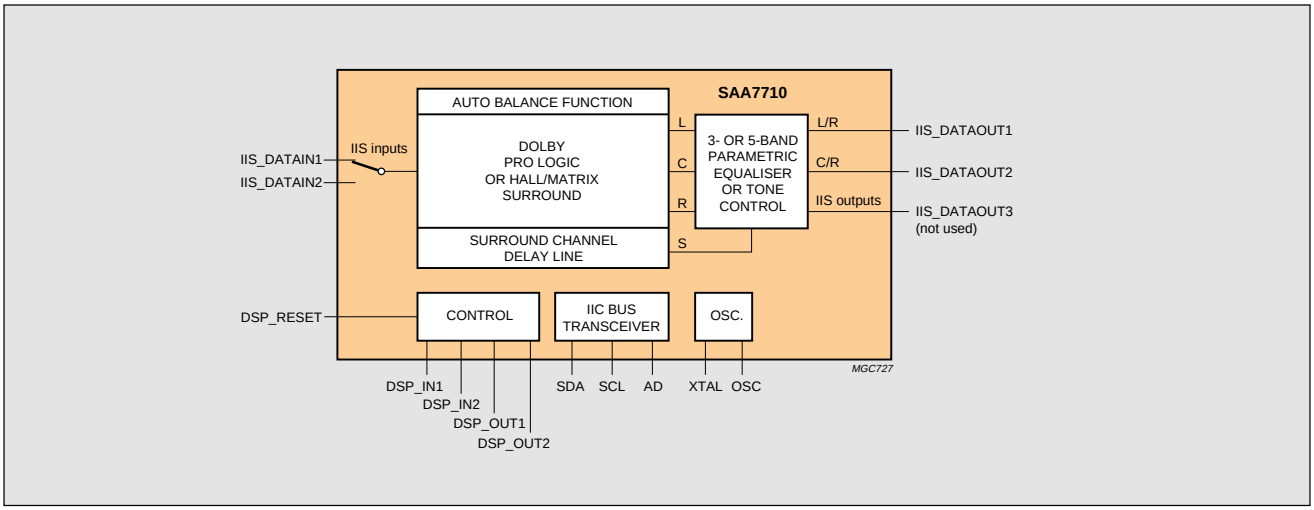
- **Adaptive matrix**
- **7 kHz low-pass filters**
- **Adjustable delay for surround channel**
- **Modified Dolby B noise reduction**
- **Noise sequencer**
- **Output volume control**
- **Automatic balance and master level control with DC-offset filter**
- **Hall and matrix surround sound functions**
- **Optional clock divider for crystal oscillator**
- **I²C-bus mode control**
- **Centre mode control**
- **2 stereo I²S digital input channels**
- **2 stereo I²S digital output channels**

This is a high-quality audio-performance add-on digital signal processor. It comprises all the necessary features on chip for complete Dolby Surround Pro Logic sound.

In addition, the device also incorporates either:
- 3-band parametric equalizer on main channels left, centre, right (f_s = 44.1 kHz), or
- 5-band parametric equalizer on main channels left, centre, right (f_s = 32 kHz), or
- tone control (bass/treble) on all four output channels (f_s = 44.1 kHz)

These features can be used to replicate surround sound as an alternative to Dolby Pro Logic, or when the input is non-Dolby surround coded.

QUICK REFERENCE DATA	
Supply voltage	4.5 to 5.5 V
4-channel active surround sound	20 to 20 000 Hz
On-chip delay line (f_s =44.1 kHz)	≤45 ms
Package	SO32



TDA1315H

Digital audio input/output circuit (DAIO)

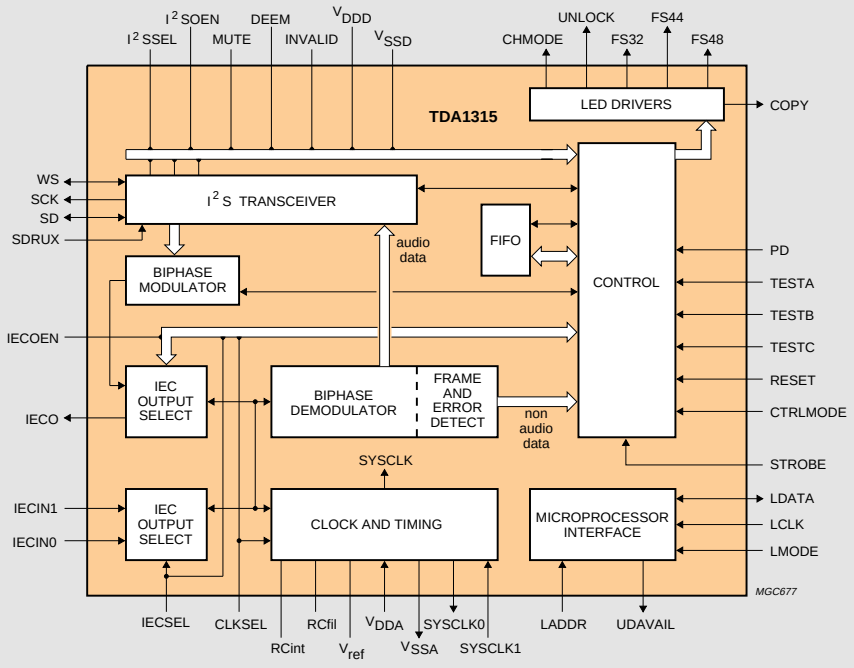
- **Transceiver for SPDIF/IEC958 encoded signals**
- **Highly sensitive input for transformer-coupled links**
- **TTL level input for optical links**
- **Built-in IEC input selector**
- **Built-in IEC feed-through function**
- **Automatic sample frequency detection**
- **System clock recovery from input signal**
- **Error detection and concealment**
- **PLL lock detection in transmit mode**
- **Serial audio interface conforms to I²S format**
- **Auxiliary I²S input for ADC**
- **Audio output selector**
- **Microprocessor-controlled and stand-alone modes**
- **128-byte buffer for user data**
- **Bytewise exchange of user data with microprocessor**
- **Decoding of Compact Disc subcode Q-channel data**
- **Support for Serial Copy Management System (SCMS)**
- **LED drive capability (sample frequency and error indication)**
- **Pin-selectable device address for microprocessor interface**

This is a completely integrated CMOS transceiver for biphase-mark encoded digital audio signals that conform to the SPDIF (Sony Philips Digital Interface) and IEC958 interface standards (consumer mode).

In the receiver mode, the IC adjusts automatically to one of the three standardized sample frequencies (32 kHz for digital satellite signals, 44.1 kHz for compact disc signals, or 48 kHz for digital audio tape signals), decodes the input signal, and separates the audio and control data. A clock signal of $256f_s$ or $384f_s$ is generated to serve as a master clock signal for the digital audio system.

In the transmitter mode, the IC multiplexes the audio, control and user data and encodes them for subsequent transmission via a cable or optical link.

QUICK REFERENCE DATA	
Supply voltage	3.4 to 5.5 V
Operating temperature range	–40 to +85 °C
Package	SQFP44



TDA1373H

General digital input (GDIN) circuit with filters

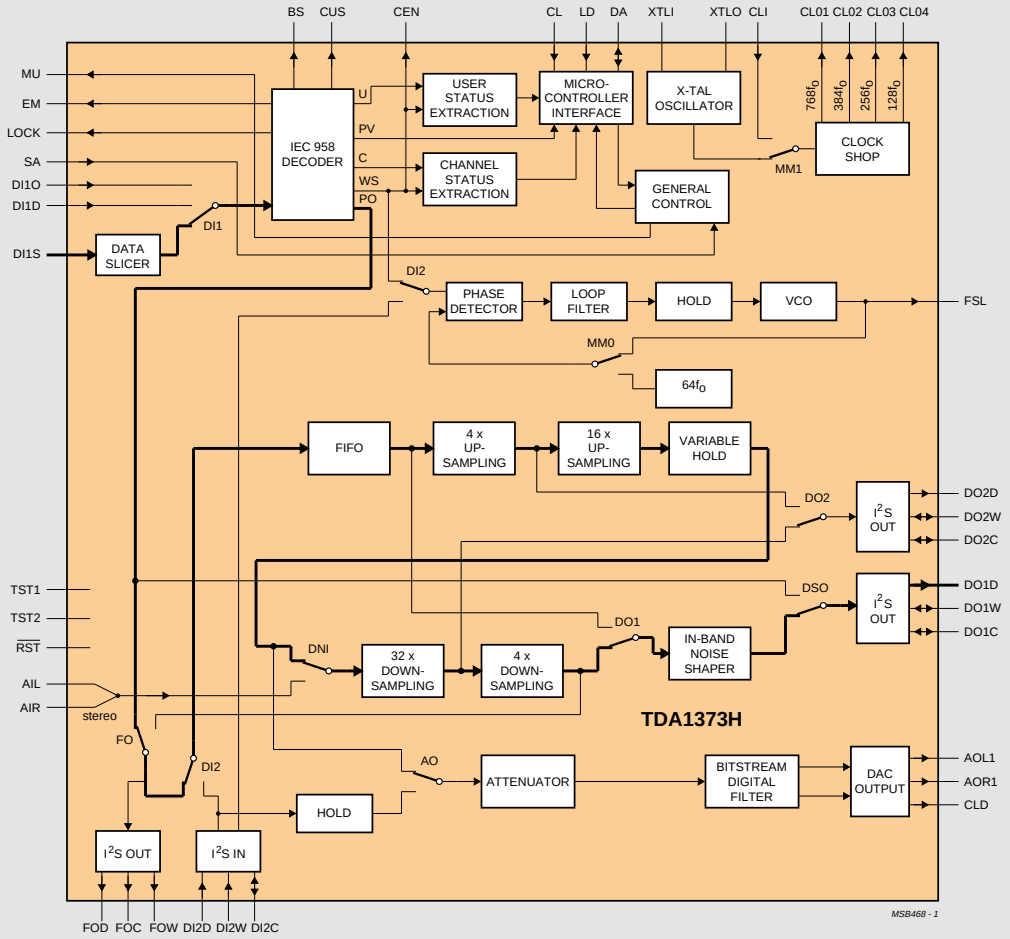
- **Fabricated in 0.8 μm double-metal CMOS**
- **Four operating modes (SRC, AD/DA, SLAVE-VCO, SLAVE-VCXO)**
- **Full digital sampling rate conversion (SRC) over a wide range of input sampling rates**
- **Fast and automatic detection and locking to the input sampling rate with continuous tracking**
- **Digital PLL with adaptive bandwidth which removes jitter on the digital audio input**
- **Audio outputs soft muted during loop acquisition**
- **Full linear-phase processing based on all-FIR filtering**
- **On-chip fully-digital IEC958 demodulator for digital input signals (AES/EBU or SPDIF format)**
- **Extended input sampling frequency range**
- **IEC958 Channel Status (CS) and User Channel (UC) outputs**
- **On-chip CS and/or UC demodulation and buffering (consumer and professional format)**
- **Dedicated sub-code processing for CD**
- **Final output quantization to 16/18/20 bits with optional in-audio-band noise shaping**
- **Bitstream input and output for coupling to 1-bit ADC and DAC**
- **I^2S and Japanese serial input formats supported for SRC and DAC functions**
- **I^2S and Japanese serial output formats supported for SRC and ADC functions**
- **I^2S and Japanese 4× oversampled serial output available for SRC and ADC functions**
- **8-bit digital gain/attenuation control**
- **Switchable DSP interface (I^2S input and output) for additional audio processing**
- **Additional clock outputs available at 768, 384, 256 and 128f_s out**
- **3-line serial microcontroller interface compatible with Philips CD I.C. protocol (HCL)**

In the SRC (Sample Rate Conversion) mode, this very versatile IC can perform high-quality sample rate conversion of digital audio signals. I reads several serial input formats and includes a Audio Digital Input Circuit (ADIC) for input signals in the IEC958 format (also known as AES/EBU or SPDIF signals). An internal PLL removes excessive jitter from the incoming digital audio signals without the need for analog loop electronics. In-audio-band noise shaping can limit the standard 20-bit output word to 16 or 18 bits.

In the AD/DA mode, the on-chip digital filters can be used for bitstream A/D and D/A conversion.

In the slave-VCO and slave-VCXO modes. the internal PLL can be reconfigured to operate in a slave mode wherein the IC is locked to the incoming sampling rate.

QUICK REFERENCE DATA	
Supply voltage range ($f_{s\ out}$ = 44.1 kHz)	4.75 to 5.5 V
Total supply current ($f_{s\ out}$ = 44.1 kHz)	166 mA
Total power dissipation ($f_{s\ out}$ = 44.1 kHz)	830 mW
SRC THD + N over the 0 to 20 kHz band (1 kHz, 20 bits input and output)	–113 dB
SRC THD + N over the 0 to 20 kHz band (1 kHz, 16 bits input and output)	–95 dB
Pass-band ripple for up-sampling and down-sampling filters	>±0.004 dB
Selectable stop-band suppression for 64× up-sampling filters	70 to 50 dB
Stop-band suppression for 128× down-sampling filters	80 dB
Maximum output sample frequency	55 kHz
AC input voltage at IEC input (DIIS)	0.2 Vp-p
Package	QFP64


BS
CUS
CEN
CL
LD
DA
XTLI
XTLO
CLI
CL01 CL02 CL03 CL04
MU
EM
LOCK
SA
DI1O
DI1D
DI1S
IEC 958 DECODER
U
PV
C
WS
PO
USER STATUS EXTRACTION
CHANNEL STATUS EXTRACTION
MICRO-CONTROLLER INTERFACE
X-TAL OSCILLATOR
768f0
384f0
256f0
128f0
CLOCK SHOP
MM1
GENERAL CONTROL
DI1
DATA SLICER
DI2
PHASE DETECTOR
LOOP FILTER
HOLD
VCO
FSL
MM0
64f0
FIFO
4 x UP-SAMPLING
16 x UP-SAMPLING
VARIABLE HOLD
DO2
I2S OUT
DO2D
DO2W
DO2C
TST1
TST2
RST
AIL
AIR
stereo
FO
DSO
DO1
DNI
32 x DOWN-SAMPLING
4 x DOWN-SAMPLING
IN-BAND NOISE SHAPER
I2S OUT
DO1D
DO1W
DO1C
TDA1373H
AO
ATTENUATOR
BITSTREAM DIGITAL FILTER
DAC OUTPUT
AOL1
AOR1
CLD
HOLD
I2S OUT
I2S IN
FOD FOC FOW DI2D DI2W DI2C
MSB468 - 1

APPENDICES

DOCUMENTATION

Datasheets

A datasheet or preliminary technical information on most of the devices in this Designer's Guide is available in PDF format for downloading from our WWW site (http://www.semiconductors.philips.com/). Data Handbooks and loose leaf data sheets of recently released ICs are also available. Please contact your local Philips sales office for more information (see address list on the back cover of this brochure).

Relevant Data Handbooks

IC01: Semiconductors for Radio and Audio Systems	9397 750 01121
IC12: I^2C Peripherals	9397 750 00306
IC22: Multimedia ICs	9397 750 01061

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Relevant Designer's Guides

Compact Disc designer's guide	9397 750 00952
Multimedia PC designer's guide	9397 750 00726
Digital Media Broadcast designer's guide	9397 750 02396
Portable and home hi-fi/radio designer's guide	9397 750 00907
Analog and digitally-enhanced TV designer's guide	9397 750 02692
Car radio designer's guide	9397 750 02687

Application and Lab. reports relating to stereo audio ADCs and DACs

TDA1541A stereo 16-bit D to A converter for medium and high-end performance digital audio applications	9398 074 30011
TDA1547 TOP-GRADE STEREO BITSTREAM DAC	nba/an9006
Application and performance of the SAA7360 bitstream audio ADC	JRA/AN93001
Application and performance of the SAA7366 bitstream audio ADC	JRA/AN93003
Application and performance of TDA1545(T): continuous calibration audio DAC	NBA/AN9101
Single active stage 3rd-order I-to-V filtering for low-end current output DACs	NBA/AN9107
TDA1547 top-grade stereo bitstream digital-to-analog converter	NBA/AN9006
Bitstream digital audio reconstruction system	NBA/AN9303
A printed-circuit board for the combination of TDA1307 bitstream digital filter and TDA1547 bitstream DAC	NBA/AN9305
Audio performance measurements on bitstream unicon I featuring TDA1315, TDA1307 and TDA1547	NBA/AN9307
A PCB for the TDA1305T digital filter and bitstream/continuous calibration DAC	NBA/AN9311
TDA1306T/TDA1386T noise shaping filter DAC	NBA/AN9312
Audio performance measurements on bitstream Unicon I featuring TDA1315, TDA1307 and TDA1547	NBA/AN9308
Supplement: Bitstream Unicon II digital audio converter	NBA/AN9310
TDA1548T(Z): low-power, low-voltage headphone filter DAC	NBA/AN9507
TDA1309H low-voltage low-power stereo bitstream ADC/DAC	NBA/AN9510
Application and performance of the SAA7360GP/M3 bitstream audio ADC (Version 1.0)	AN96009

Brochures relating to stereo audio ADCs and DACs

Bitstream conversion	9398 379 80011
USB audio ICs; UDA1321T USB DAC	9397 750 01072
TDA1547 stereo top-performance bitstream digital-to-analog converter IC	–

Application notes related to dedicated signal processors

Outline of a layer-1 MPEG decoder using the SAA2520	SAU/AN92012
An economical low-pass filter design for a 1-bit DAC in the MPEG Audio Decoder SAA2502H	AN96082
User Guide for the SAA2502H Demonstration Unit (Version 1.0)	AN96019
MPEG layer-1 audio compression/decompression chip-set	SAU/AN92013
Design of 8 kHz-LP and 4 kHz-LP measurement filters	AT-AU18/89
User guide for the Philips SAA2520/SAA2521 MPEG audio layer 1 demonstration unit	SAU/AN93016
SAA7274 Audio Digital Input Circuit for converting SPDIF signals into I^2S signals	NBA/AN9102
TDA1315 Digital Audio Input/Output circuit	NBA/AN9309

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INDEX OF TYPE NUMBERS